Low Distortion, Precision, Wide Bandwidth Op Amp

AD9617

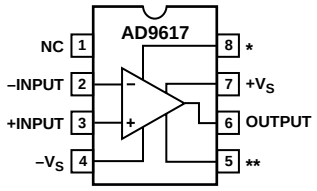
FEATURES

Usable Closed-Loop Gain Range: ±1 to ±40
Low Distortion: –67 dBc (2nd) at 20 MHz
Small Signal Bandwidth: 190 MHz (A_V = +3)
Large Signal Bandwidth: 150 MHz at 4 V p-p
Settling Time: 10 ns to 0.1%; 14 ns to 0.02%
Overdrive and Output Short Circuit Protected
Fast Overdrive Recovery
DC Nonlinearity 10 ppm

APPLICATIONS

Driving Flash Converters
D/A Current-to-Voltage Converters
IF, Radar Processors
Baseband and Video Communications
Photodiode, CCD Preamps

PIN CONFIGURATION



NC = NO CONNECT
*OPTIONAL $+V_S$ **OPTIONAL $-V_S$

NOTE:
FOR BEST SETTLING TIME AND DISTORTION PERFORMANCE, USE OPTIONAL SUPPLY CONNECTIONS. PERFORMANCE INDICATED IN SPECIFICATIONS IS BASED ON SUPPLY CONNECTIONS TO THESE PINS.

GENERAL DESCRIPTION

The AD9617 is a current feedback amplifier which utilizes a proprietary architecture to produce superior distortion and dc precision. It achieves this along with fast settling, very fast slew rate, wide bandwidth (both small signal and large signal) and exceptional signal fidelity. The device achieves –67 dBc 2nd harmonic distortion at 20 MHz while maintaining 190 MHz small signal and 150 MHz large signal bandwidths.

These attributes position the AD9617 as an ideal choice for driving flash ADCs and buffering the latest generation of DACs. Optimized for applications requiring gain between ±1 to ±15, the AD9617 is unity gain stable without external compensation.

The AD9617 offers outstanding performance in high fidelity, wide bandwidth applications in instrumentation ranging from network and spectrum analyzers to oscilloscopes, and in military systems such as radar, SIGINT and ESM systems. The superior slew rate, low overshoot and fast settling of the AD9617 allow the device to be used in pulse applications such as communications receivers and high speed ATE. Most monolithic op amps suffer in these precision pulse applications due to slew rate limiting.

The AD9617J operates over the range of 0°C to +70°C and is available in either an 8-lead plastic DIP or an 8-1ead plastic small outline package (SOIC).

REV. B

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AD9617–SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltages ($\pm V_S$) . . . . . +7 V
Common-Mode Input Voltage . . . . . ±Vs
Differential Input Voltage . . . . . 3 V
Continuous Output Current[2] . . . . . 70 mA
Operating Temperature Ranges
  AD9617JN/JR . . . . . 0°C to +70°C
Storage Temperature
  AD9617JN/JR . . . . . –65°C to +125°C
Junction Temperature[3]
  AD9617JN/JR . . . . . +150°C
Lead Soldering Temperature (10 Seconds) . . . . . +300°C

NOTES
[1] Absolute maximum ratings are limiting values to be applied individually and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.
[2] Output is short circuit protected to ground, but not to supplies. Continuous short circuit to ground may affect device reliability.
[3] Typical thermal impedances (part soldered onto board):
Plastic DIP: θ_{JA} = 140°C/W; θ_{JC} = 30°C/W. SOIC Package: θ_{JA} = 155°C/W; θ_{JC} = 40°C/W.

DC ELECTRICAL CHARACTERISTICS (Unless otherwise noted, A_V = +3; $\pm V_S$ = ±5 V; R_F = 400 Ω; R_{LOAD} = 100 Ω)

Parameter	Conditions	Temp	Test Level	AD9617JN/JR Min	AD9617JN/JR Typ	AD9617JN/JR Max	AD9617AQ/SQ* Min	AD9617AQ/SQ* Typ	AD9617AQ/SQ* Max	AD9617BQ/TQ* Min	AD9617BQ/TQ* Typ	AD9617BQ/TQ* Max	Units
Input Offset Voltage[1, 2]		+25°C	I	–1.1	+0.5	+2.2	–1.1	+0.5	+2.2	+0.0	+0.5	+1.35	mV
Input Offset Voltage TC[2]		Full	IV	–4	+3	+25	–4	+3	+25	–4	+3	+25	µV/°C
Input Bias Current[2]													
Inverting		+25°C	I	–50	0	+50	–50	0	+50	–25	0	+25	µA
Noninverting		+25°C	I	–25	+5	+35	–25	+5	+35	–15	+5	+20	µA
Input Bias Current TC[2]													
Noninverting		Full	IV	–50	+30	+125	–50	+30	+125	–50	+30	+125	nA/°C
Inverting		Full	IV	–50	+50	+150	–50	+50	+150	–50	+50	+150	nA/°C
Input Resistance													
Noninverting		+25°C	V		60			60			60		kΩ
Input Capacitance													
Noninverting		+25°C	V		1.5			1.5			1.5		pF
Common-Mode Input Range[3]	$T = T_{MAX}$	←	II	±1.4	±1.5		±1.4	±1.5		±1.4	±1.5		V
	$T = T_{MIN}$ to +25°C	←	II	±1.7	±1.8		±1.7	±1.8		±1.7	±1.8		V
Common-Mode Rejection Ratio[4]	$T = T_{MIN}$ to T_{MAX}	←	II	44	48		44	48		44	48		dB
	$T = T_{MIN}$ to +25°C	←	II	48	51		48	51		48	51		dB
Power Supply Rejection Ratio	ΔV_S = ±5%	Full	II	48	51		48	51		48	51		dB
Open Loop Gain													
T_O	At DC	+25°C	V		500			500			500		kΩ
Nonlinearity	At DC	+25°C	IV		10			10			10		ppm
Output Voltage Range		+25°C	II	±3.4	±3.8		±3.4	±3.8		±3.4	+3.8		V
Output Impedance	At DC	+25°C	V		0.07			0.07			0.07		Ω
Output Current (50 Ω Load)	$T = +25°C$ to T_{MAX}	←	II	60			60			60			mA
	$T = T_{MIN}$	←	II	50			50			50			mA

NOTES
*Pending obsoletion: last-time buy October 25, 1999.
[1]Measured with respect to the inverting input.
[2]Typical is defined as the mean of the distribution.
[3]Measured in voltage follower configuration.
[4]Measured with V_{IN} = +0.25 V.

Specifications subject to change without notice.

AC ELECTRICAL CHARACTERISTICS (Unless otherwise noted, A_V = +3; $\pm V_S$ = ±5 V; R_F = 400 Ω; R_{LOAD} = 100 Ω)

Parameter	Conditions	Temp	Test Level	AD9617JN/JR Min	AD9617JN/JR Typ	AD9617JN/JR Max	AD9617AQ/SQ* Min	AD9617AQ/SQ* Typ	AD9617AQ/SQ* Max	AD9617BQ/TQ* Min	AD9617BQ/TQ* Typ	AD9617BQ/TQ* Max	Units
FREQUENCY DOMAIN													
Bandwidth (–3 dB)													
Small Signal	$V_{OUT} \le 2$ V p-p	Full	II	135	190		145	190		145	190		MHz
Large Signal	V_{OUT} = 4 V p-p	Full	IV		150		115	150		115	150		MHz
Bandwidth Variation vs. A_V	A_V = –1 to ±15	+25°C	V		40			40			40		MHz
Amplitude of Peaking (<50 MHz)	T = T_{MIN} to +25°C	←	II		0			0	0.3		0	0.3	dB
	T = T_{MAX}	←	II		0			0	0.6		0	0.6	dB
Amplitude of Peaking (>50 MHz)	T = T_{MIN} to +25°C	←	II		0			0	0.8		0	0.8	dB
	T = T_{MAX}	←	II		0			0	1.0		0	1.0	dB
Amplitude of Roll-Off (<60 MHz)		Full	II		0.1			0.1	0.6		0.1	0.6	dB
Phase Nonlinearity	DC to 75 MHz	+25°C	V		0.5			0.5			0.5		Degree
2nd Harmonic Distortion	2 V p-p; 4.3 MHz	Full	IV		–86	–78		–86	–78		–86	–78	dBc
	2 V p-p; 20 MHz	Full	IV		–67	–59		–67	–59		–67	–59	dBc
	2 V p-p; 60 MHz	Full	II		–51	–43		–51	–43		–51	–43	dBc
3rd Harmonic Distortion	2 V p-p; 4.3 MHz	Full	IV		–83	–75		–83	–75		–83	–75	dBc
	2 V p-p; 20 MHz	Full	IV		–69	–61		–69	–61		–69	–61	dBc
	2 V p-p; 60 MHz	Full	II		–54	–46		–54	–46		–54	–46	dBc
Input Noise Voltage	10 MHz	+25°C	V		1.2			1.2			1.2		nV/√Hz
Inverting Input Noise Current	10 MHz	+25°C	V		29			29			29		pA/√Hz
Average Equivalent Integrated													
Input Noise Voltage	0.1 MHz to 200 MHz	+25°C	V		55			55			55		µV, rms
TIME DOMAIN													
Slew Rate	V_{OUT} = 4 V Step	Full	IV		1400		1100	1400		1100	1400		V/µs
Rise/Fall Time													
V_{OUT} = 2 V Step		Full	IV		2.0			2.0	2.5		2.0	2.5	ns
V_{OUT} = 4 V Step	T = +25°C to T_{MAX}	←	IV		2.4			2.4	3.3		2.4	3.3	ns
V_{OUT} = 4 V Step	T = T_{MIN}	←	IV		2.4			2.4	3.5		2.4	3.5	ns
Overshoot	V_{OUT} = 2 V Step	Full	IV		3			3	14		3	14	%
Settling Time													
To 0.1%	V_{OUT} = 2 V Step	Full	IV		10			10	15		10	15	ns
To 0.02%	V_{OUT} = 2 V Step	Full	IV		14			14	23		14	23	ns
To 0.1%	V_{OUT} = 4 V Step	Full	IV		11			11	16		11	16	ns
To 0.02%	V_{OUT} = 4 V Step	Full	IV		16			16	24		16	24	ns
2× Overdrive Recovery to													
±2 mV of Final Value	V_{IN} = 1.7 V Step	+25°C	V		50			50			50		ns
Propagation Delay		+25°C	V		2			2			2		ns
Differential Gain[1]		Full	V		<0. 01			<0. 01			<0 .01		%
Differential Phase[1]		Full	V		0.01			0.01			0.01		Degree
POWER SUPPLY REQUIREMENTS													
Quiescent Current													
$+I_S$		Full	II		34	48		34	48		34	48	mA
$-I_S$		Full	II		34	48		34	48		34	48	mA

NOTES

*Pending obsoletion: last-time buy October 25, 1999.

[1]Frequency = 4.3 MHz; R_L = 150 Ω; A_V = +3.

Specifications subject to change without notice.

EXPLANATION OF TEST LEVELS

Test Level

I - 100% production tested.

II - 100% production tested at +25°C and sample tested at specified temperatures. AC testing of J grade devices done on sample basis.

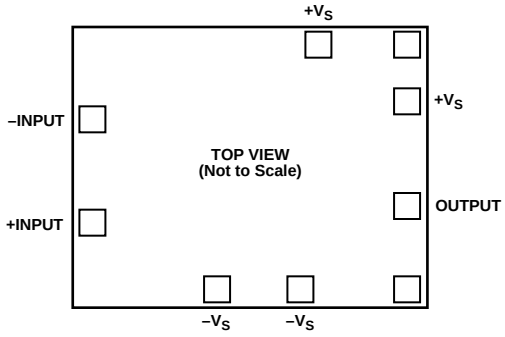
III - Sample tested only.

IV - Parameter is guaranteed by design and characterization testing.

V - Parameter is a typical value only.

VI - All devices are 100% production tested at +25°C. 100% production tested at temperature extremes for extended temperature devices; sample tested at temperature extremes for commercial/industrial devices.

DIE CONNECTIONS



DIE SIZE = 53 × 67 × 15 mils

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9617JN	0°C to +70°C	Plastic DIP	N-8
AD9617JR	0°C to +70°C	SOIC	SO-8
AD9617JR-REEL	0°C to +70°C	13" Tape and Reel	SO-8

Typical Performance Characteristics (A_V = +3; $\pm V_S$ = ±5 V; R_F = 400 V, unless otherwise noted)

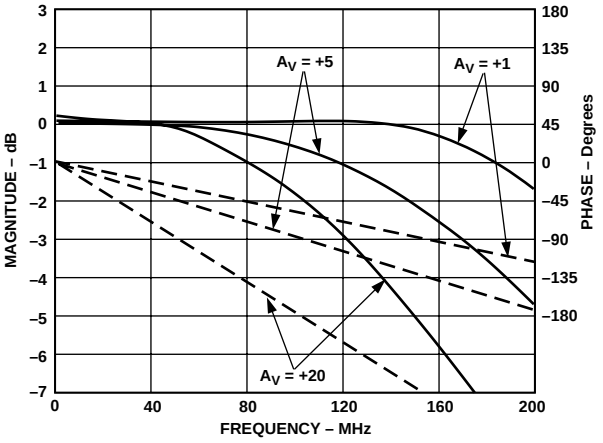


Figure 1. Noninverting Frequency Response

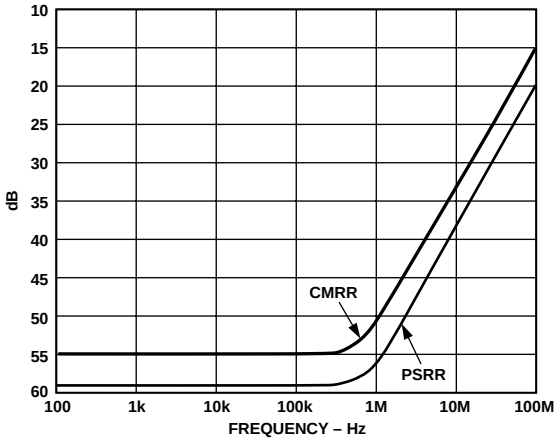


Figure 4. CMRR and PSRR

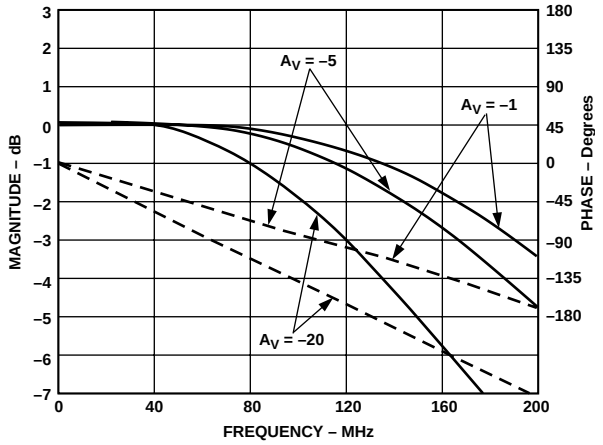


Figure 2. Inverting Frequency Response

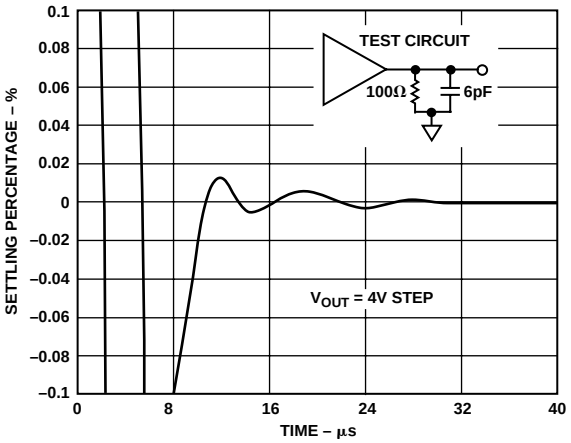


Figure 5. Settling Time

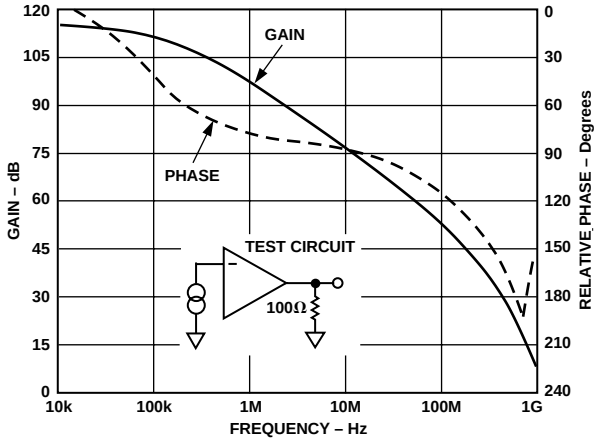


Figure 3. Open Loop Transimpedance Gain [T(s) Relative to 1 Ω]

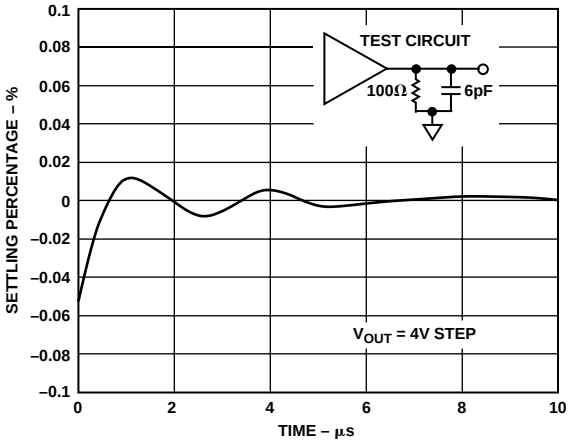


Figure 6. Long Term Settling Time

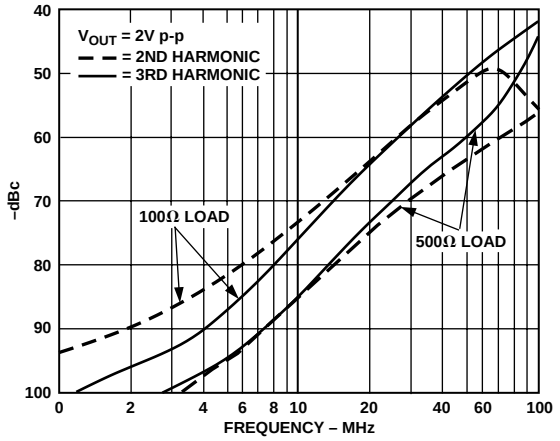


Figure 7. Harmonic Distortion

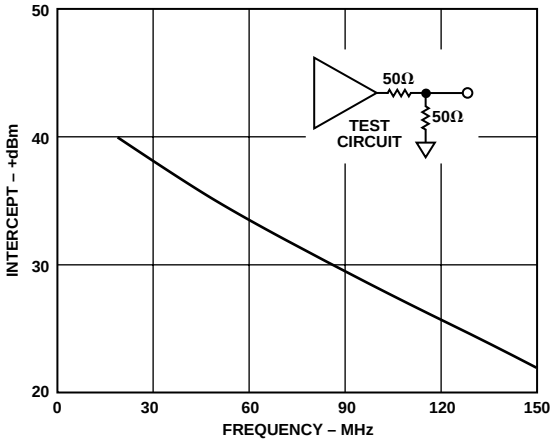


Figure 10. Intermodulation Distortion (IMD)

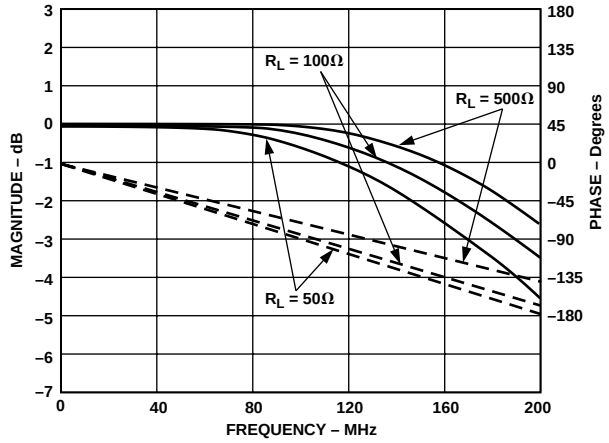


Figure 8. Frequency Response vs. R_{LOAD}

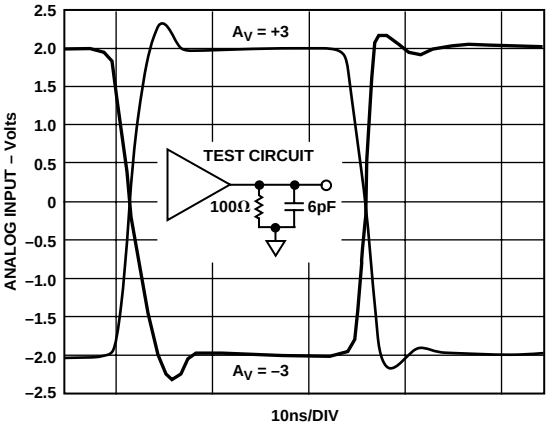


Figure 11. Large Signal Pulse Response

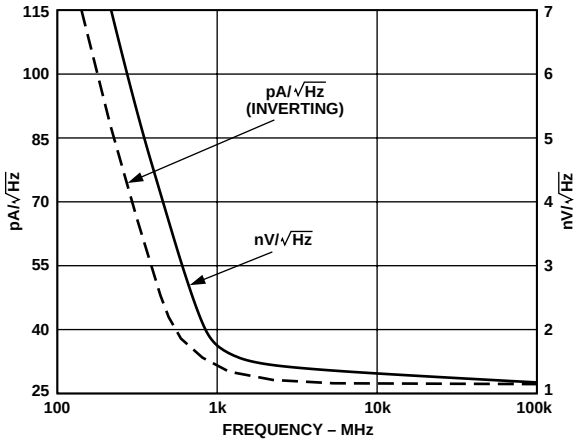


Figure 9. Equivalent Input Noise

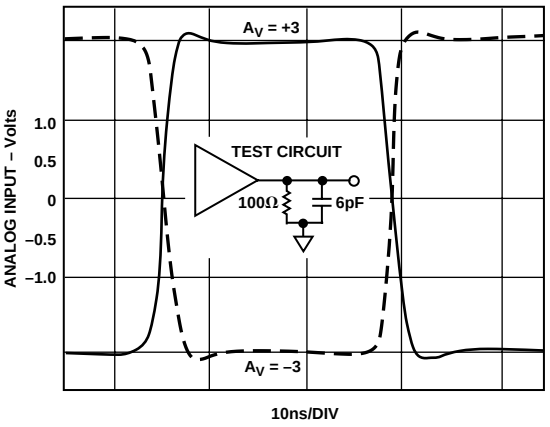


Figure 12. Small Signal Pulse Response

THEORY OF OPERATION

The AD9617 has been designed to combine the key attributes of traditional "low frequency" precision amplifiers with exceptional high frequency characteristics that are independent of closed-loop gain. Previous "high frequency" closed-loop amplifiers have low open loop gain relative to precision amplifiers. This results in relatively poor dc nonlinearity and precision, as well as excessive high frequency distortion due to open loop gain roll-off.

Operational amplifiers use two basic types of feedback correction, each with advantages and disadvantages. Voltage feedback topologies exhibit an essentially constant gain bandwidth product. This forces the closed-loop bandwidth to vary inversely with closed-loop gain. Moreover, this type design typically slew rate limits in a way that causes the large signal bandwidth to be much lower than its small signal characteristics.

A newer approach is to use current feedback to realize better dynamic performance. This architecture provides two key attributes over voltage feedback configurations: (1) avoids slew rate limiting and therefore large signal bandwidth can approach small signal performance; and (2) low bandwidth variation versus gain settings, due to the inherently low open loop inverting input resistance (R_S).

The AD9617 uses a new current feedback topology that overcomes these limitations and combines the positive attributes of both current feedback and voltage feedback designs. These devices achieve excellent high frequency dynamics (slew, BW and distortion) along with excellent low frequency linearity and good dc precision.

DC GAIN CHARACTERISTICS

A simplified equivalent schematic is shown below. When operating the device in the inverting mode, the input signal error current (I_E) is amplified by the open loop transimpedance gain (T_O). The output signal generated is equal to $T_O \times I_E$. Negative feedback is applied through R_F such that the device operates at a gain (G) equal to $-R_F/R_I$.

Noninverting operation is similar, with the input signal applied to the high impedance buffer (noninverting) input. As before, an output (buffer) error current (I_E) is generated at the low impedance inverting input. The signal generated at the output is fed back to the inverting input such that the external gain is $(1 + R_F/R_I)$. The feedback mechanics are identical to the voltage feedback topology when exact equations are used.

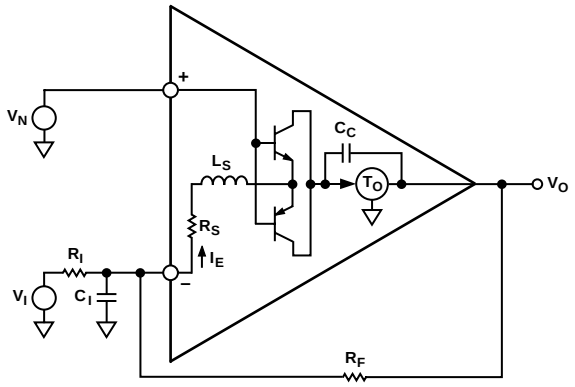


Figure 13. Equivalent Circuit

The major difference lies in the front end architecture. A voltage feedback amplifier has symmetrical high resistance (buffered) inputs. A current feedback amplifier has a high noninverting resistance (buffered) input and a low inverting (buffer output) input resistance. The feedback mechanics can be easily developed using current feedback and transresistance open loop gain T(s) to describe the I/O relationship. (See typical specification chart.)

DC closed-loop gain for the AD9617 can be calculated using the following equations:

$$G = \frac{V_O}{V_I} \approx \frac{-R_F / R_I}{1 + 1/LG} \quad \text{inverting} \qquad (1)$$

$$G = \frac{V_O}{V_N} \approx \frac{1 + R_F / R_I}{1 + 1/LG} \quad \text{noninverting} \qquad (2)$$

$$\text{where} \quad \frac{1}{LG} \approx \frac{R_S \left(R_F + R_S \parallel R_I\right)}{T(s)\left(R_S \parallel R_I\right)} \qquad (3)$$

Because the noninverting input buffer is not ideal, input resistance R_S (at dc) is gain dependent and is typically higher for noninverting operation than for inverting operation. R_S will approach the same value (≈7 Ω) for both at input frequencies above 50 MHz. Below the open loop corner frequency, the noninverting R_S can be approximated as:

$$R_S\left(noninverting\right) \approx 7 + \frac{T(s)}{A_O} = 7 + \left.\frac{T_O}{A_O}\right|_{dc} \qquad (4)$$

where: A_O = *Open Loop Voltage Gain* ≈ G × 600

Inverting R_S below the open loop corner frequency can be approximated as:

$$R_S\left(inverting\right) \approx 7 + \frac{T(s)}{A_O} = 7 + \left.\frac{T_O}{A_O}\right|_{dc} \qquad (5)$$

where: A_O = 40,000.

The AD9617 approaches this condition. With $T_O = 1 \times 10^6$ Ω, R_L = 500 Ω and R_S = 25 Ω (dc), a gain error no greater than 0.05% typically results for G = –1 and 0.15% for G = –40. Moreover, the architecture linearizes the open loop gain over its operating voltage range and temperature resulting in ≥16 bits of linearity.

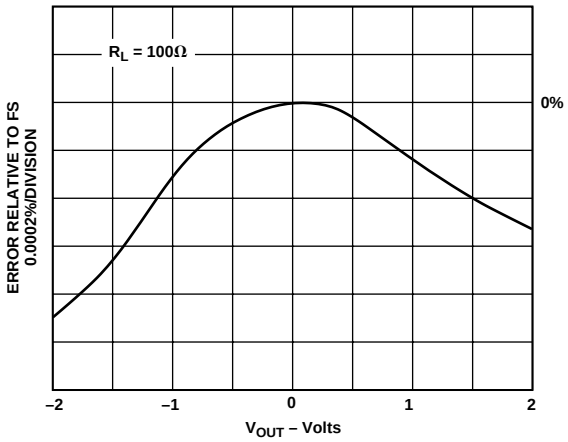


Figure 14. DC Nonlinearity vs. V_{OUT}

AC GAIN CHARACTERISTICS

Closed-loop bandwidth at high frequencies is determined primarily by the roll-off of T(s). But circuit layout is critical to minimize external parasitics which can degrade performance by causing premature peaking and/or reduced bandwidth.

The inverting and noninverting dynamic characteristics are similar. When driving the noninverting input, the inverting input capacitance (C_I) will cause the noninverting closed-loop bandwidth to be higher than the inverting bandwidth for gains less than two (2). In the remaining cases, inverting and noninverting responses are nearly identical.

For best overall dynamic performance, the value of the feedback resistor (R_F) should be 400 ohms. Although bandwidth reduces as closed-loop gain increases, the change is relatively small due to low equivalent series input impedance, Z_S. (See typical performance charts.) The simplified equations governing the device's dynamic performance are shown below.

Closed-Loop Gain vs. Frequency:
(noninverting operation)

$$\frac{V_O}{V_I} \approx \frac{1+\frac{R_F}{R_I}}{s\tau\left(1+\frac{R_S}{R_I}\right)+1} \tag{6}$$

where: $\tau = R_F \times C_C = 0.9\ ns$ (R_F = 400 Ω)

$$Slew\ Rate \approx \frac{\Delta V_O}{R_F K C_C} \times e^{-\tau/R_F K C_C} \tag{7}$$

where: $K = 1+\frac{R_S}{R_I}$

Increasing Bandwidth at Low Gains

By reducing R_F, wider bandwidth and faster pulse response can be attained beyond the specified values, although increased overshoot, settling time and possible ac peaking may result. As a rule of thumb, overshoot and bandwidth will increase by 1% and 8%, respectively, for a 5% reduction in R_F at gains of ±10. Lower gains will increase these sensitivities.

Equations 6 and 7 are simplified and do not accurately model the second order (open loop) frequency response term which is the primary contributor to overshoot, peaking and nonlinear bandwidth expansion. (See Open Loop Bode Plots.) The user should exercise caution when selecting R_F values much lower than 400 Ω. Note that a feedback resistor must be used in all situations, including those in which the amplifier is used in a noninverting unity gain configuration.

Increasing Bandwidth at High Gains

Closed loop bandwidth can be extended at high closed loop gain by reducing R_F. Bandwidth reduction is a result of the feedback current being split between R_S and R_I. As the gain increases (for a given R_F), more feedback current is shunted through R_I, which reduces closed loop bandwidth (see Equation 6). To maintain specified BW, the following equations can be used to approximate R_F and R_I for any gain from ±1 to ±15.

$$R_F = 424 \pm 8\ G \tag{8}$$

(+ for inverting and – for noninverting)

$$R_I \approx \frac{424-8\ G}{G-1} \quad \text{(noninverting)} \tag{9}$$

$$R_I \approx \frac{424+8\ G}{G-1} \quad \text{(inverting)} \tag{10}$$

G = *Closed Loop Gain.*

Bandwidth Reduction

The closed loop bandwidth can be reduced by increasing R_F. Equations 6 and 7 can be used to determine the closed loop bandwidth for any value R_F. Do not connect a feedback capacitor across R_F, as this will degrade dynamic performance and possibly induce oscillation.

DC Precision and Noise

Output offset voltage results from both input bias currents and input offset voltage. These input errors are multiplied by the noise gain term ($1 + R_F/R_I$) and algebraically summed at the output as shown below.

$$V_O = V_{IO} \times \left(1+\frac{R_F}{R_I}\right) \pm IBn \times R_N \times \left(1+\frac{R_F}{R_I}\right) \pm IBi \times R_F \tag{11}$$

Since the inputs are asymmetrical, IBi and IBn do not correlate. Canceling their output effects by making $R_N = R_F \| R_I$ will not reduce output offset errors, as it would for voltage feedback amplifiers. Typically, IBn is 5 µA and V_{IO} is +0.5 mV (I sigma = 0.3 mV), which means that the dc output error can be reduced by making $R_N \approx 100\ \Omega$. Note that the offset drift will not change significantly because the IBn TC is relatively small. (See specification table.)

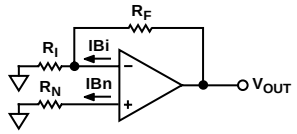


Figure 15. Output Offset Voltage

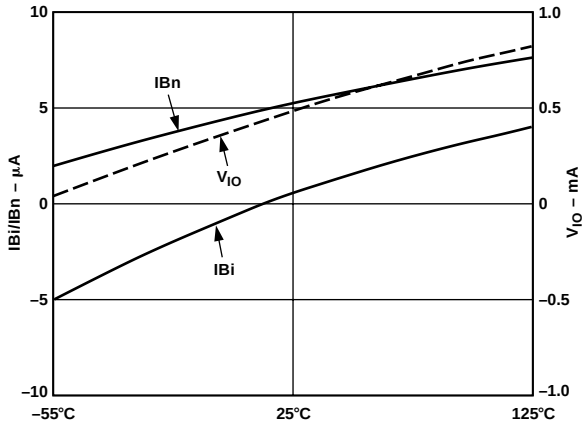


Figure 16. DC Accuracy

The effective noise at the output of the amplifier can be determined by taking the root sum of the squares of Equation 11 and applying the spectral noise values found in the typical graph section. This applies to noise from the op amp only. Note that both the noise figure and equivalent input offset voltages improve as the closed loop gain is increased (by keeping R_F fixed and reducing R_I with R_N = 0 Ω).

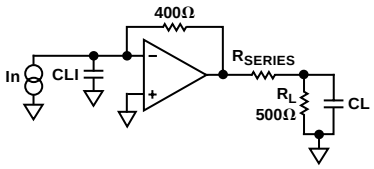


Figure 17. Capacitive Load Figure

Capacitive Load Considerations

Due to the low inverting input resistance (R_S) and output buffer design, the AD9617 can directly handle input and/or output load capacitances of up to 20 pF. See the chart below.

A small series resistor can be used at the output of the amplifier and outside of the feedback loop to facilitate driving larger capacitive loads or for obtaining faster settling time. For capacitive loads above 20 pF, R_{SERIES} should be considered.

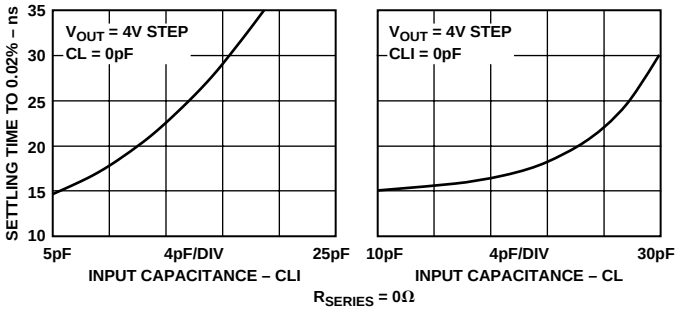


Figure 18. Input/Output Capacitance Comparisons

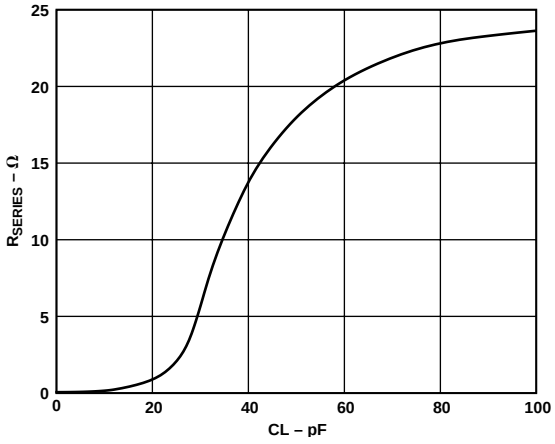


Figure 19. Recommended R_{SERIES} vs. CL

APPLYING THE AD9617

The superior frequency and time domain specifications of the AD9617 make it an obvious choice for driving flash converters and buffering the outputs of high speed DACs. Its outstanding distortion and noise performance make it well suited as a driver for analog to digital converters (ADCs) with resolutions as high as 16 bits.

Typical circuits for inverting and noninverting applications are shown in Figures 20 and 21.

Closed-loop gain for noninverting configurations is determined by the value of RI according to the equation:

$$G = 1 + \frac{R_F}{R_I} \tag{12}$$

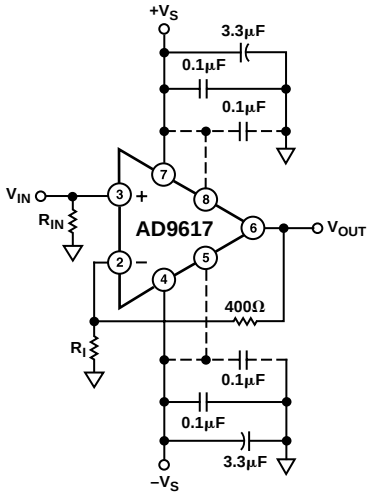


Figure 20. Noninverting Operation

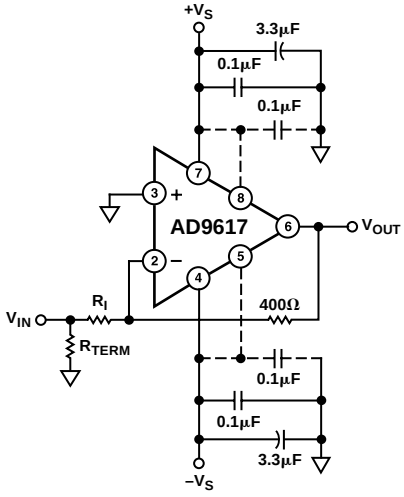


Figure 21. Inverting Operation

LAYOUT CONSIDERATIONS

As with all high performance amplifiers, printed circuit layout is critical in obtaining optimum results with the AD9617. The ground plane in the area of the amplifier should cover as much of the component side of the board as possible. Each power supply trace should be decoupled close to the package with at least a 3.3 µF tantalum and a low inductance, 0.1 µF ceramic capacitor.

All lead lengths for input, output and the feedback resistor should be kept as short as possible. All gain setting resistors should be chosen for low values of parasitic capacitance and inductance, i.e., microwave resistors and/or carbon resistors.

Stripline techniques should be used for lead lengths in excess of one inch. Sockets should be avoided if possible because of their stray inductance and capacitance.

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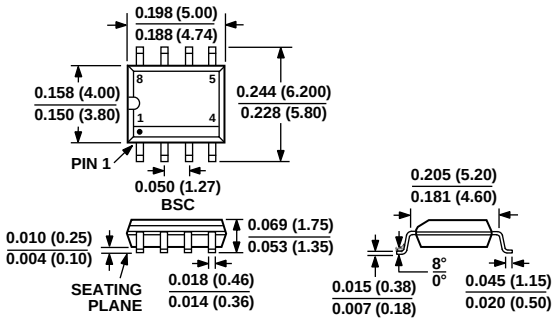
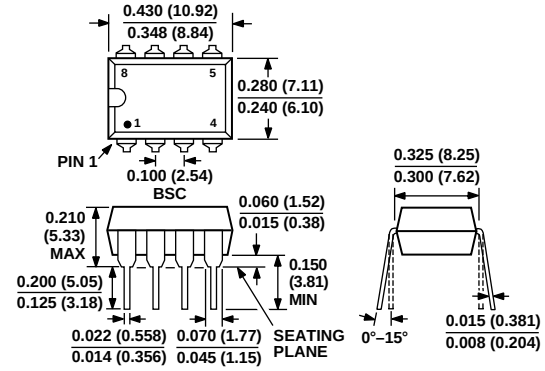
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

Small Outline Package (SO-8)



Plastic DIP (N-8)



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