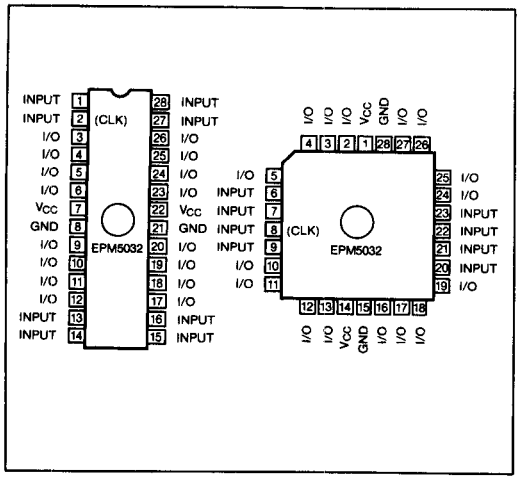
32 MACROCELL HIGH DENSITY MAX EPLD — EPM5032

FEATURES

- Erasable, User-Configurable, High-Density replacement for TTL and 74HC logic.
- Advanced 0.8 micron CMOS EPROM technology.
- High speed tpd = 20ns and 83MHz clock frequencies.
- Programmable I/O architecture providing up to 24 inputs and 16 outputs.
- 32 Macrocells providing registered and combinatorial operation.
- Programmable registers configurable as Flow Through Latches or D, T, SR or JK flip-flops with individual Asynchronous Clear and Preset controls.
- Independent clocking of all registers or synchronous registered operation from one system clock.
- Expander Product Term Array supplies 64 additional product terms to all macrocells or 32 additional latches.
- 100% generically testable—provides 100% programming yield.
- Programmable security bit protects proprietary designs.
- MAX+PLUS software supports hierarchical Graphic Editor, State Machine, Truth Table and Boolean Equation entry.
- Available in a 28 pin, 300 mil, DIP and a 28 pin J-leaded chip carrier.

CONNECTION DIAGRAM



GENERAL DESCRIPTION

The Altera EPM5032 is a User-Configurable, High-Performance MAX (Multiple Array MatriX) CMOS EPLD. The EPM5032 is a high-density replacement for SSI and MSI TTL and 74HC logic. In addition, it can integrate multiple 20 and 24 pin PLD devices. Available in a 28 pin, 300 mil DIP or in a 28 pin J-leaded chip carrier, the EPM5032 accomodates designs with up to 24 inputs and 16 outputs.

The EPM5032 architecture is based on one flexible Logic Array Block (LAB), shown in Figure 1, that encompasses three components: the Macrocell Array, the Expander Product Term Array, and the I/O Control block.

The Macrocell Array contains 32 MAX macrocells. Each macrocell has a programmable AND, fixed OR array and a configurable register that provides D, T, JK, SR, or Flow Through Latch operation with independent, programmable clock options. All macrocells can implement active high or active low combinatorial, registered and latched operations. Each macrocell contains 8 product terms for logic implementation, but if needed, the Expander Product Term array will supply additional product terms.

The Expander Product Term Array is a programmable AND structure with inversion that supplies the Macrocell Array with up to 64 additional product terms or with up to 32 asynchronous latches.

The EPM5032 has 16 bidirectional I/O pins that can be configured for dedicated input, dedicated output, or bidirectional operation. Each I/O pin has a dedicated feedback path to the Global Bus. The I/O Control block contains 16 tristate buffers which can be programmed to decouple the pins from the Macrocell Array thus separating the macrocell and I/O pin feedbacks. Macrocells and I/O pins have separate feedbacks, enabling the user to bury macrocell logic and retain the pins for input. This feature is called "dual feedback."

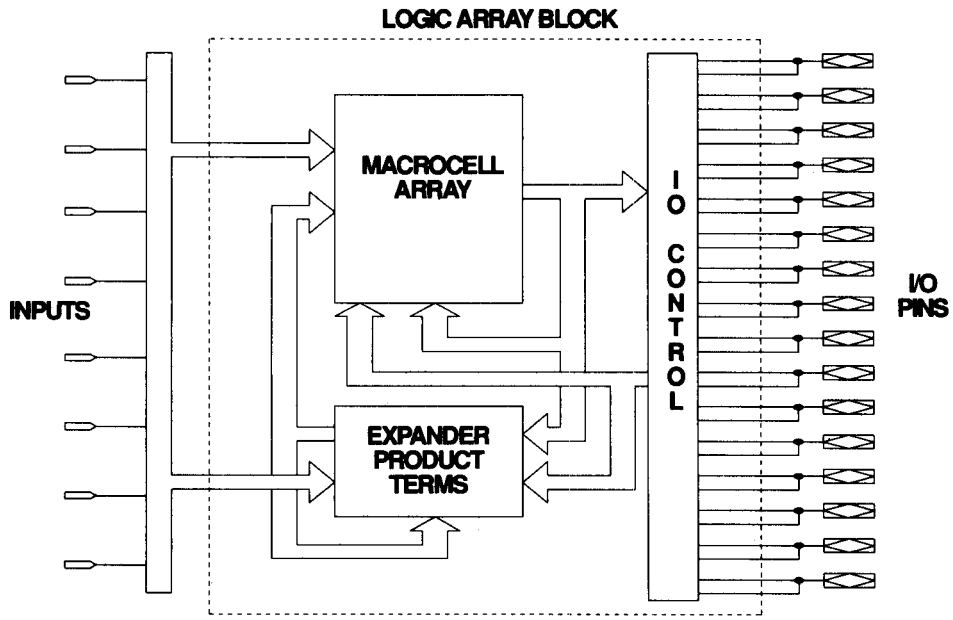
EPM5032 designs are developed and programmed using Altera's MAX+PLUS (Programmable Logic User System) PC-based development system. MAX+PLUS is a complete development system offering high level entry tools, design

PRELIMINARY DATA

NOTICE: THIS IS NOT A FINAL SPECIFICATION. SOME PARAMETRIC LIMITS ARE SUBJECT TO CHANGE.

REV. 1.0

Figure 1. EPM5032 Logic Array Block Diagram



compilation, full timing simulation and device programming. Design entry is via the hierarchical Graphic Editor, State Machine, Truth Table and Boolean Equation entries. The Compiler performs automatic error detection and location, to simplify design rule checking and error correction. Logic minimization and synthesis are automatically performed to optimize all submitted designs. The Compiler also places the optimized logic, generating a resource utilization report and a device programming file. An EPM5032 may then be programmed using standard Altera programming hardware and the appropriate EPM5032 adaptor.

FUNCTIONAL DESCRIPTION

Figure 1 shows the block diagram of the EPM5032. Externally, the device provides 8 dedicated data inputs and has 16 bidirectional I/O pins which can be configured for input, output, or bidirectional operation.

Internally, the EPM5032 has one LAB. The LAB contains a Macrocell Array with 32 macrocells, an Expander Product Term Array with 64 product terms, and a user-configurable I/O Control block. All internal signals, as well as input and feedback signals, are connected to the EPM5032 Global Bus.

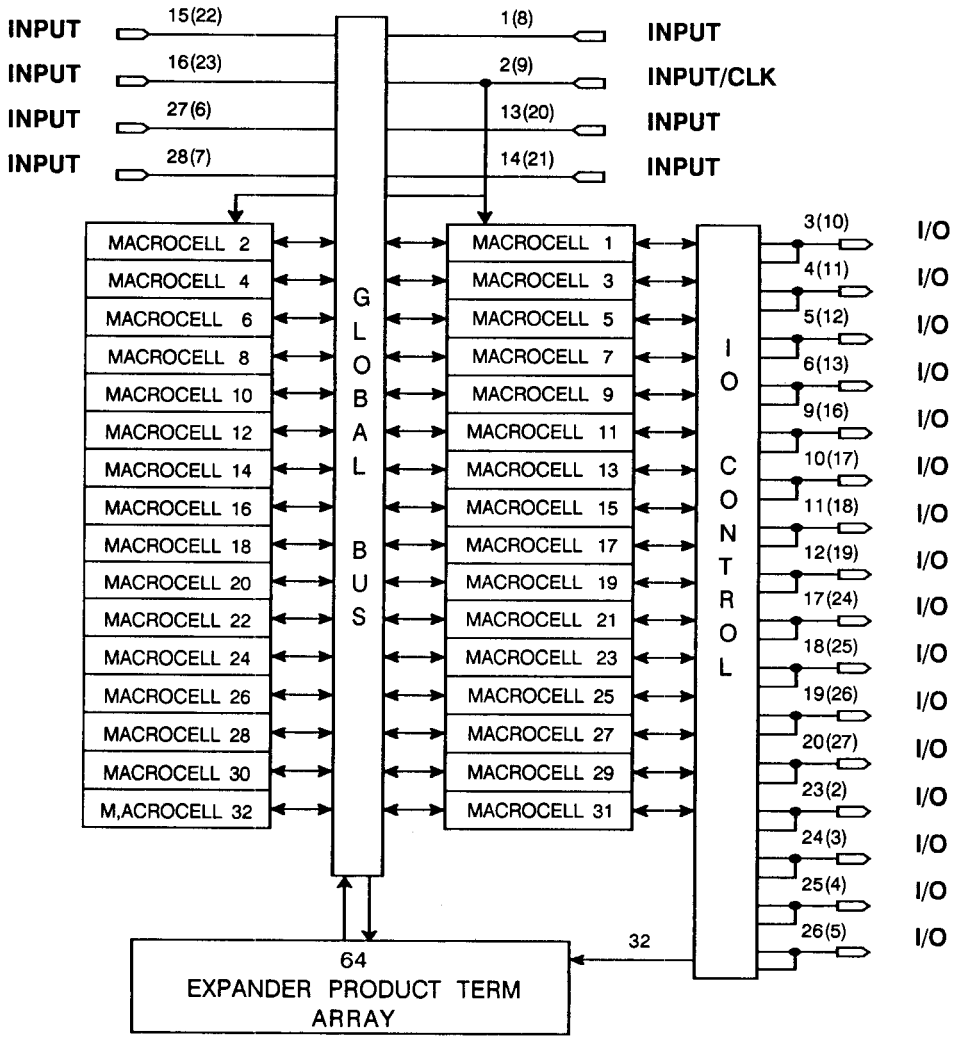
MACROCELL ARRAY

The Macrocell Array shown in Figure 2 contains 32 MAX macrocells. All macrocells are interconnected via the Global Bus which routes all input, I/O feedback, macrocell feedback, and Expander Product Term signals between the macrocells. The I/O and macrocell feedbacks are independent of each other, as all macrocells are "buried" or disjoint from the I/O pins. Each macrocell remains buried, until the user specifies an I/O connection; Up to 16 macrocells may be connected to the I/O pins.

Each EPM5032 macrocell, shown in Figure 3, contains a programmable AND, fixed OR array and an user-configurable register architecture. Inputs into the AND array come from the true and complemented signals of the 8 dedicated inputs, 32 macrocell and 16 I/O pins. Inputs also come from the Expander Product Term Array, providing 32 to 64 additional inputs. (See Expander Product Term Array).

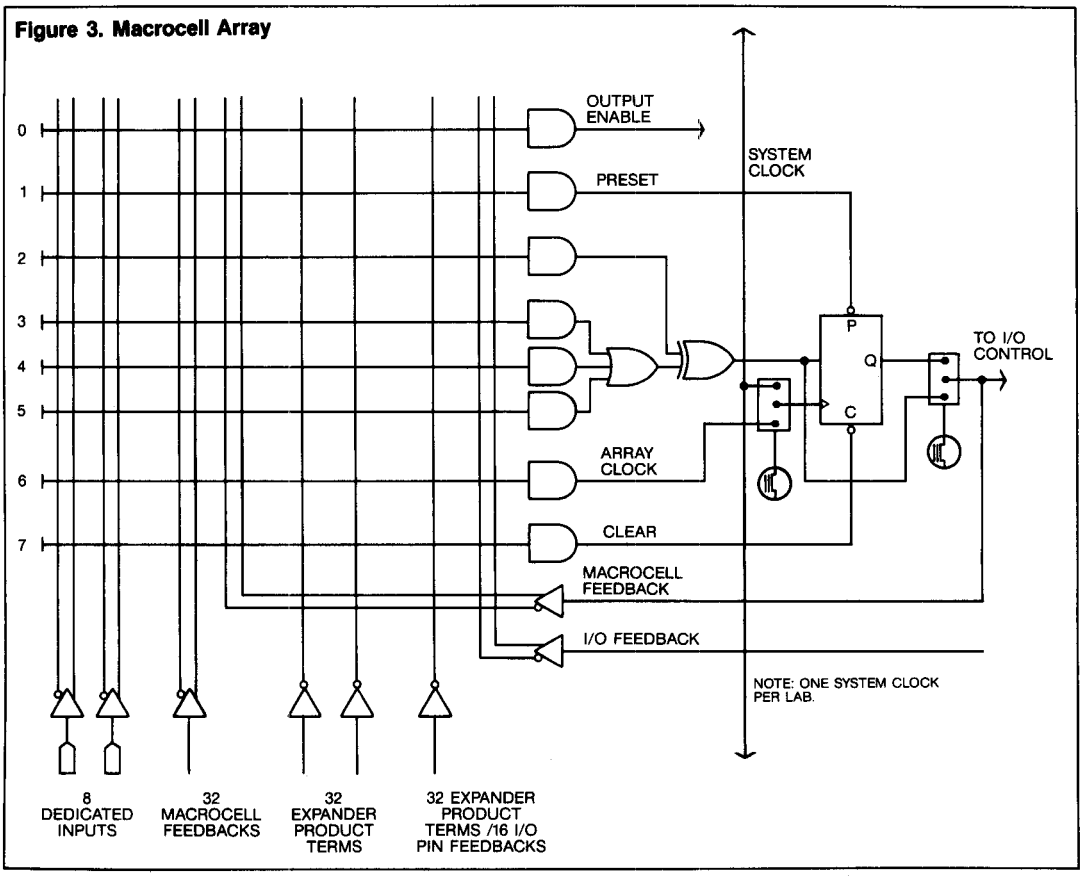
The AND-OR array implements all combinatorial logic such as decoders, adders, and the simpler NAND, NOR, OR, AND functions. The array is an EPROM array which provides 8 product terms per macrocell. Three product terms are dedicated for

Figure 2. EPM5032 Block Diagram



NOTE: Figures within ( ) pertain to J-leaded packages.

Figure 3. Macrocell Array



logic implementation and the remainder for control logic. These 3 terms are OR'ed together forming a Sum-Of-Product result that is then XOR'ed with a single product term. This single term controls logic inversion. By setting this inversion term to logic true or "1", the Sum-Of-Product result is always complemented providing active low operation.

In addition, the XOR gate provides the ability to implement arithmetic or mutually exclusive logic functions such as MUX'es, with a minimal use of Expander Product Terms or additional macrocells. MAX+PLUS software automatically programs the single product term to represent the mutually exclusive logic via logic synthesis. The XOR result is then routed to the programmable register for registered function or by-passed for combinatorial logic. The combinatorial or registered output then feeds back to the Global Bus and may also be connected to the I/O block for output.

PROGRAMMABLE REGISTER

Each of the EPM5032's 32 registers may be individually configured as D, T, JK, or SR flip-flops, or as a Flow Through Latches, as in Figure 4. All registers may be clocked with the system clock input from Pin 2 (DIP) or Pin 9 (Jlead), or independently clocked by a dedicated product term within its macrocell AND array; All registers are positive edge triggered.

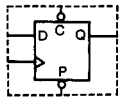
Each register also supports both Asynchronous Preset and Clear. As shown in Figure 3, product terms in the AND array generate the control logic for these operations. Single product terms control the active low Asynchronous Clear and Asynchronous Preset.

If more product terms are required for logic implementation of control logic, additional product terms may be taken from the Expander Product Term Array; each macrocell treats the Expander Product Terms as data inputs.

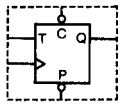
EXPANDER PRODUCT TERM ARRAY

The EPM5032's Expander Product Term Array, shown in Figure 5, supplies up to 64 Expander Product Terms available for use by all macrocells. The Expander Product Term Array is an AND-INVERT array where each product term is a function of the array inputs. Expander Product Term Array inputs are the true and complemented signals of all dedicated inputs, macrocell feedbacks, I/O pins, and Expander Product Terms. For

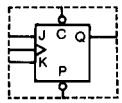
Figure 4. Register Configuration



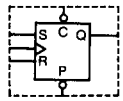
CK	D	P	C	Q	Q+
X	X	0	1	X	1
X	X	1	0	X	0
↑	0	1	1	X	0
↑	1	1	1	X	1



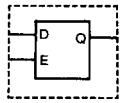
CK	T	P	C	Q	Q+
X	X	0	1	X	1
X	X	1	0	X	0
↑	0	1	1	0	0
↑	0	1	1	1	1
↑	1	1	1	0	1
↑	1	1	1	1	0



CK	J	K	P	C	Q	Q+
X	X	X	0	1	X	1
X	X	X	1	0	X	0
↑	0	0	1	1	A	A
↑	0	1	1	1	X	0
↑	1	0	1	1	X	1
↑	1	1	1	1	A	A'



CK	S	R	P	C	Q	Q+
X	X	X	0	1	X	1
X	X	X	1	0	X	0
↑	0	0	1	1	A	A
↑	0	1	1	1	X	0
↑	1	0	1	1	X	1



D	E	Q	Q+
X	0	A	A
0	1	X	0
1	1	X	1

↑ Rising Edge Triggered

every I/O pin configured as an input, two Expander product terms are removed.

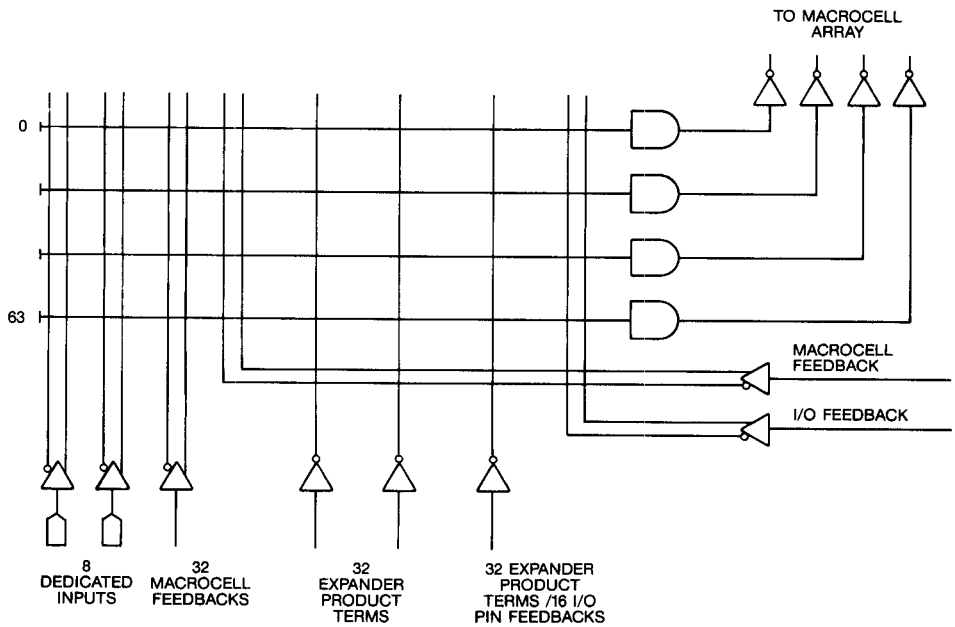
The Expander Product Term Array feeds the Global Bus. Logic implemented with Expanders may be shared by all macrocells, thereby saving resources. Expanders also route back into the Expander Product Term Array, enabling Expanders to be cross-coupled for asynchronous latches. The EPM5032 Expanders can implement up to 32 Latches. This allows Expanders to augment either combinatorial or registered logic as needed by each design.

I/O CONTROL BLOCK

The I/O Control Block contains 16 programmable tristate buffers and I/O pins with optional feedbacks as shown in Figure 6. Each I/O pin may be configured for dedicated input, or a macrocell may be connected to an I/O pin allowing the pin to be used as a dedicated output, or as a bi-directional pin. For outputs, the tristate control can be permanently enabled by setting it to logic "1" or controlled by logic. As shown in Figure 3, one product term within the macrocell is the Output Enable control for the tristate output buffer; this product term stays unused if the macrocell remains buried.

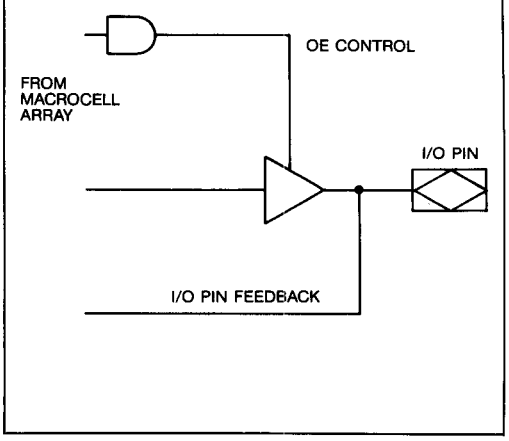
I/O feedback and the macrocell feedback are

Figure 5. Expander Product Term Array



independent and global. This architectural feature called "dual feedback" enables the I/O pin to be used as an output, and as an input when the Output Enable is disabled. Input pin and register intensive applications such as state machines may successfully use "dual feedback", storing state variables in buried macrocells while using the I/O pins for both inputs and outputs.

Figure 6. I/O Control Block



DESIGN RECOMMENDATION

Operation of devices described herein with conditions above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure to absolute maximum rating condition for extended periods may affect device reliability. These devices contain circuitry to protect the input against damage to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

For proper operation, input and output pins must be constrained to the range GND (Vin or Vout) Vcc. Unused inputs must be tied to an appropriate logic level either Vcc or GND). Each set of Vcc and GND pins must be shorted together directly at the device. Power supply decoupling capacitors of at least 0.2 microfarad must be connected between Vcc and GND. for the most effective decoupling, each Vcc pin should be separately decoupled to GND, directly at the device.

As with any CMOS device, power is a function of frequency and internal nodes switching. It is recommended that current consumption be measured after the design is completed and placed in the board.

TIMING DELAYS

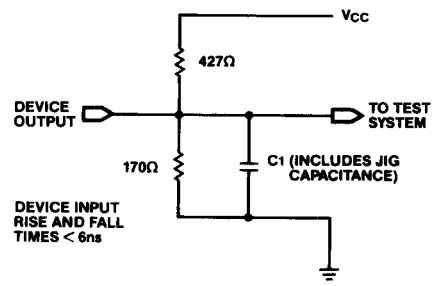
With MAX+PLUS and the EPM5032, time delays may be easily determined (See EPM5032 TIMING MODEL). The EPM5032 has fixed internal delays, allowing the user to determine the operating frequency for any design. For complete timing information, MAX+PLUS provides a complete timing simulator.

FUNCTIONAL TESTING

The EPM5032 is fully functional tested and guaranteed through complete testing of each programmable EPROM bit and all internal logic elements thus ensuring 100% programming yield.

As a result, traditional problems associated with fuse-programmed circuits are eliminated. The erasable nature of the EPM5032 allows test program patterns to be used and then erased. This facility to use application independent, general purpose tests is called generic testing and is unique among user-defined LSI logic devices.

Figure 7. AC Test Conditions



Power supply transients can affect AC measurements, simultaneous transitions of multiple outputs should be avoided for accurate measurement.
Do not attempt to perform threshold tests under AC conditions. Large amplitude, fast ground current transients normally occur as the device outputs discharge the load capacitances. These transients flowing through the parasitic inductance between the device ground pin and the test system ground can create significant reductions in observable input noise immunity.

DESIGN SECURITY

The EPM5032 contains a programmable design security feature that controls access to the data programmed into the device. If this programmable feature is used, a proprietary design implemented in the device enables a high level of design control to be obtained since programmed data within EPROM cells is invisible. The bit that controls this function, along with all other program data, may be reset simply by erasing the device.

Figure 8. I_{CC} VS f_{MAX}

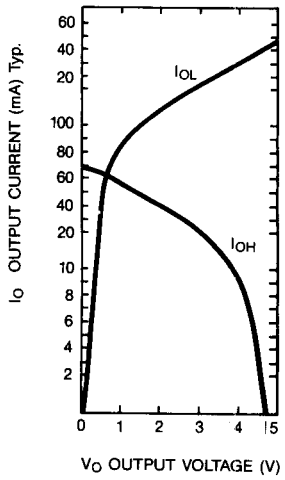
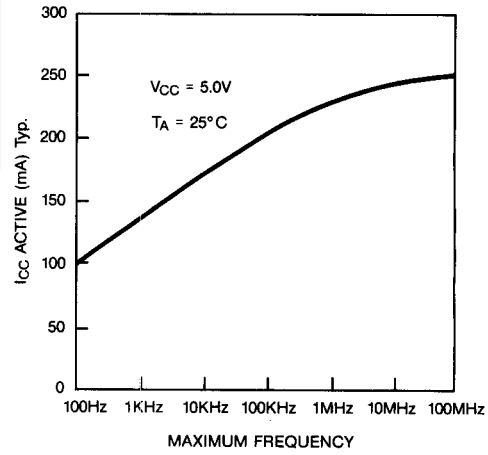


Figure 9. Output Drive Currents



MAX+PLUS SOFTWARE

DESIGN ENTRY

MAX+PLUS supports a variety of design entry methods. Boolean Equation entry is available for entering simple combinatorial logic and register functions. State Machine Entry may be used to enter designs in a high level language syntax, as well as Truth Table inputs. Since MAX EPLDs offer the designer large amount of logic capability, Altera has created a hierarchical Graphic Editor to ease the design process.

MAX+PLUS will also accept various 3rd party netlists, as well as existing EPLD designs implemented with Altera's A+PLUS or Intel's iPLDs or iPLDS II systems.

The hierarchical Graphic Editor is a mouse driven, multiple windowed enviroment utilizing pop-up menus for entering commands.

The hierarchical Graphic Editor supports design entry with TTL symbols selected from the MAX+PLUS MacroFunction library of over 100 7400 series and special purpose MacroFunctions, as well as gate-level primitives such as NAND, AND, OR gates and registers; All MacroFunctions have been optimized for the MAX architecture. Since the Graphic Editor supports hierarchies, designers may also define and store multi-leveled, custom MacroFunctions.

An additional feature of the hierarchical Graphic Editor is the Delay Predictor. This tool provides instant feedback concerning the timing of the processed design. By placing the mouse cursor at the starting point and then at the end point, the user may determine the shortest and longest propagation delays of speed critical paths. The result of the calulation is displayed at the bottom of the Graphic Editor. This is a valuable tool for design debugging and documentation.

DESIGN COMPILER

The MAX+PLUS Design Processor offers automatic error checking, logic synthesis and minimization, and automatic design fitting. The Compiler first extracts the netlist from the submitted design; at this time, the Compiler flattens the design and checks it for design rules violations. If errors are found, the Compiler features automatic error location, finding and highlighting the offending logic. After design rule checking, the Compiler applies sophisticated logic synthesis and minimization algorithms to delete redundant logic and reformat the design into an optimal configuration; It also automatically fits the design. MAX+PLUS then issues a fitter report, showing the design implementation and resource utilization, and produces a programming object file.

ABSOLUTE MAXIMUM RATINGS

Note: See Design Recommendations

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V_{CC}	Supply voltage	With respect to GND note (3)	-2.0	7.0	V
V_{PP}	Programming supply voltage		-2.0	13.5	V
V_I	DC INPUT voltage		-2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current			300	mA
I_{OUT}	DC OUTPUT current, per pin		-25	+25	mA
P_D	Power dissipation			1500	mW
T_{STG}	Storage temperature	No bias	-65	+150	°C
T_{AMB}	Ambient temperature	Under bias	0	+70	°C
T_j	Junction temperature	Under bias		150	°C

COMMERCIAL OPERATING RANGES

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V_{CC}	Supply Voltage		4.75	5.25	V
V_I	INPUT voltage		0	V_{CC}	V
V_O	OUTPUT voltage		0	V_{CC}	V
T_A	Operating temperature	For Commercial	0	70	°C
T_A	Operating temperature	For Industrial	N/A	N/A	°C
T_C	Case temperature	For Military	N/A	N/A	°C
T_R	INPUT rise time			500	ns
T_F	INPUT fall time			500	ns

DC OPERATING CHARACTERISTICS

(V_{CC} = 5V ±5%, T_A = 0°C to 70°C for Commercial)
Note (1)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	HIGH level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	LOW level input voltage		-0.3		0.8	V
V_{OH}	HIGH level TTL output voltage	I_{OH} = -4mA DC	2.4			V
V_{OL}	LOW level output voltage	I_{OL} = 8mA DC			0.45	V
I_I	Input leakage current	V_I = V_{CC} or GND	-10		+10	μA
I_{OZ}	3-state output off-state current	V_O = V_{CC} or GND	-40		+40	μA
I_{CC1}	V_{CC} supply current (standby)	V_I = V_{CC} or GND No load		120		mA
I_{CC3}	V_{CC} supply current	V_I = V_{CC} or GND No load, f = 1.0 MHz note (4)		125		mA

CAPACITANCE

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V f = 1.0 MHz		10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V f = 1.0 MHz		12	pF

AC CHARACTERISTICS

(V_{CC} = 5V ± 5%, T_A = 0°C to 70°C for Commercial)

			EPM5032-2			EPM5032			
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
t_{PD1}	Input to non-registered output	C_1 = 35pF		20			25		ns
t_{PD2}	I/O input to non-registered output			20			25		ns
t_{IN}	Input pad and buffer delay			6			7		ns
t_{IO}	I/O input pad and buffer delay			6			7		ns
t_{EXP}	Expander Array delay			13			16		ns
t_{LAD}	Logic Array Delay			8			11		ns
t_{LAC}	Logic Control Array Delay			6			8		ns
t_{OD}	Output buffer and pad delay	C_1 = 35pF		5			6		ns
t_{ZX}	Output buffer enable			8			10		ns
t_{XZ}	Output buffer disable	C_1 = 5pF note (2)		8			10		ns
f_{MAX}	Maximum clock frequency	note (5)		83.3			71.4		MHz
t_{SU}	Register set-up time			5			5		ns
t_{LATCH}	Flow through latch delay			1			1		ns
t_{RD}	Register delay			1			1		ns
t_{COMB}	Combinatorial delay			1			1		ns
t_H	Register hold time			8			10		ns
t_{CH}	Clock high time			6			7		ns
t_{CL}	Clock low time			6			7		ns
t_{IC}	Clock delay			8			10		ns
t_{ICS}	System clock delay			3			4		ns
t_{FD}	Feedback delay			1			1		ns
t_{PRE}	Register preset time			6			7		ns
t_{CLR}	Register clear time			6			7		ns
t_{CNT}	Minimum clock period (register output feedback to register input—internal path)			15			18		ns
f_{CNT}	Internal maximum frequency ($1/t_{CNT}$)	note (4)		66.6			55.6		MHz

Notes:
1. Typical values are for T_A = 25°C, V_{CC} = 5V.
2. Sample tested only for an output change of 500mV.
3. Minimum DC input is -0.3V. During transitions, the inputs may undershoot to 2.0V for periods less than 20ns.
4. Measured with device programmed as 32-Bit Counter.
5. f_{MAX} values shown represent the highest frequency for pipelined data.

Note:
These are typical values derived from design simulations. Call Altera Applications for the most recent values. (408) 984-2805 x102.

GRADE	AVAILABILITY
Commercial (0°C to 70°C)	EPM5032-2 EPM5032
Industrial (-40°C to 85°C)	Consult Factory
Military (-55°C to 125°C)	Consult Factory

*** The specifications noted above apply to military operating range devices. MIL-STD-883 compliant product applications are provided in military product drawings available from Altera marketing at 408/984-2805, ext. 101. These military product drawings should be used for the preparation of source control drawings.**

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Figure 10. Macrocell Delay Path

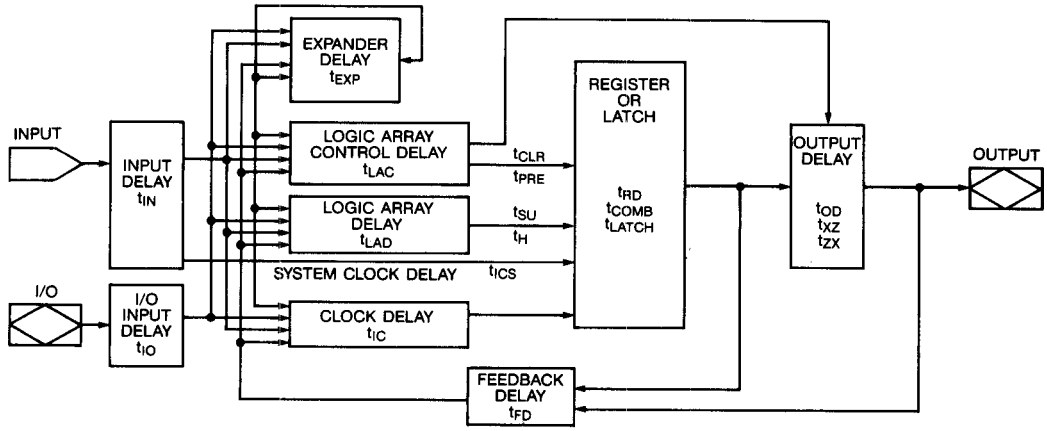
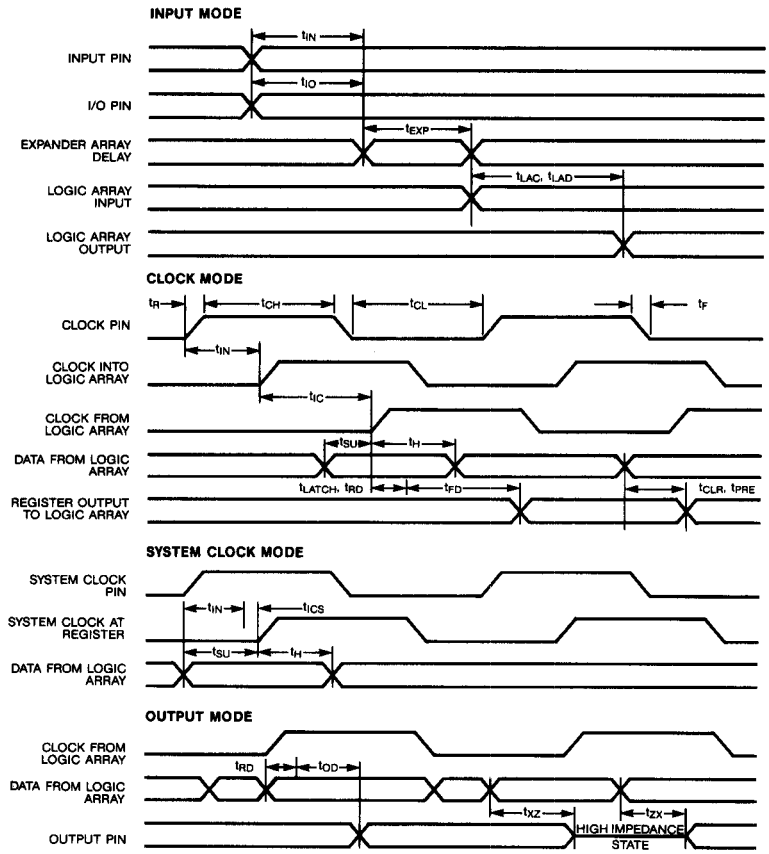


Figure 11. Switching Waveform



DESIGN SIMULATION

Verification and analysis of the completed design may be accomplished with the powerful timing simulator within MAX+PLUS. The Simulator is a interactive, event-driven simulator that yields true timing and functional characteristics of the compiled design.

Input stimulus can be defined using a straightforward vector input language, or waveforms can be directly drawn using the Graphical Waveform Editor. Outputs may also be viewed in the Waveform Editor, or hardcopy tabular and waveform files may be printed out.

The Timing Simulator offers 1/10 nanosecond resolution as well as advanced features like hold time, set-up time, and oscillation detection.

DEVICE PROGRAMMING

The EPM5032 may be programmed on IBM AT, or compatible, and PS/2 computers using Altera hardware: the LP4 or LP5 programming card, the PLE3-12A Master Programmer, and the appropriate EPM5032 adaptor. These items are included in a complete PLDS-MAX development system or may be purchased separately. MAX+PLUS software is available as part of the PLDS-MAX system or as PLS-MAX, stand alone development software package. For complete information, please consult the MAX+PLUS development system datasheet.