Report on iADC sync input problem

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GMRT Wideband Back-end is a hybrid back-end which uses ROACH (FPGA) boards with iADCs for digitisation and packetization of baseband input signals and CPU-GPUs for correlation and beamformation of the digitized data. iADC's sync input is provided GPS PPS/PPM signal as trigger for synchronization of data from all the baseband inputs. Recently, we have found that few iADCs are not passing on the PPS/PPM signal to FPGA which resulted in few ROACH boards not triggering.

In iADC, sync input (PPS/PPM) is given to input of IC SN65LVDS1 which converts the single ended input signal to differntial signal. The differential signal is passed on to FPGA through Z-DOK connector. The cause of the problem is the failure of single-ended to differential signal converter IC SN65LVDS1. On replacing the IC, the problem has been solved.

We used a Digital Storage Ocilloscope to see the voltage levels of input and outputs of IC SN65LVDS1 with ROACH board in OFF condition and with ROACH board in ON condition and with FPGA programmed with bof file which packetizes and sends the digitized data over CX4 10GbE port to CPU-GPU. An 800 MHz clock signal is given to iADC clock input and a GPS PPS signal (50% duty cycle) is given as sync input. DSO screenshots showing the voltage levels are given below. For faulty IC, a dc offset at the input can be seen and at the inverting output the voltage level is constant with no pulse.

Working IC :

ROACH board in OFF condition

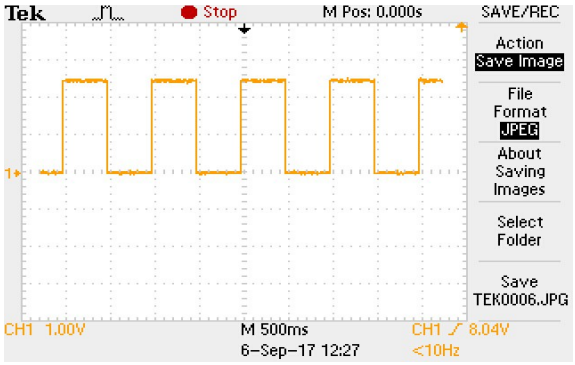

Fig 1 : Voltage level at input

ROACH board in ON condition before programming the FPGA

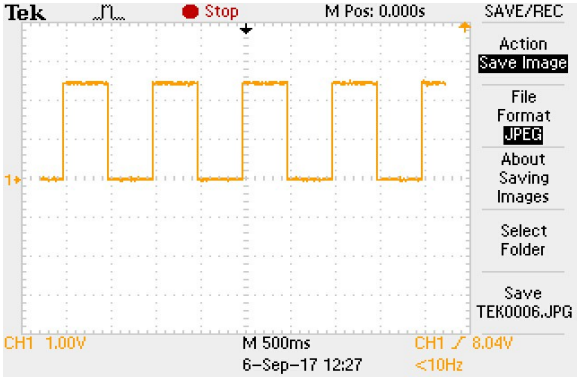

Fig 2 : Voltage level at input

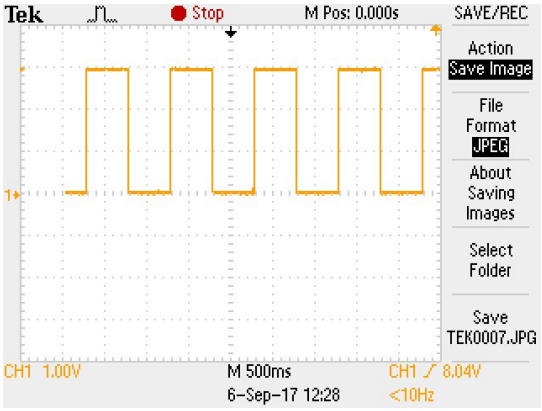

Fig 3 : Voltage level at non-inverting output

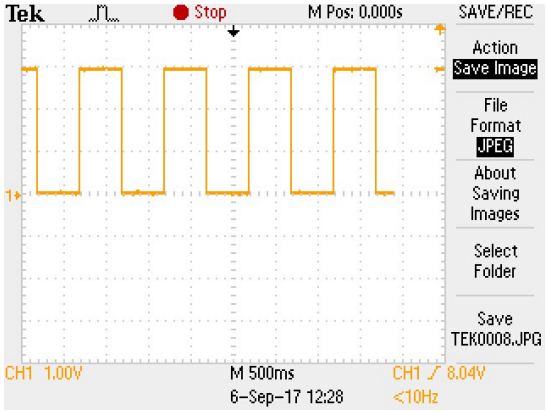

Fig 4 : Voltage level at inverting output

ROACH board in ON condition and after programming the FPGA

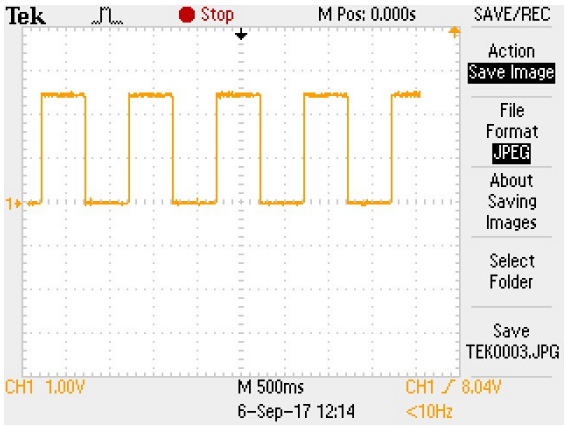

Fig 5 : Voltage level at input

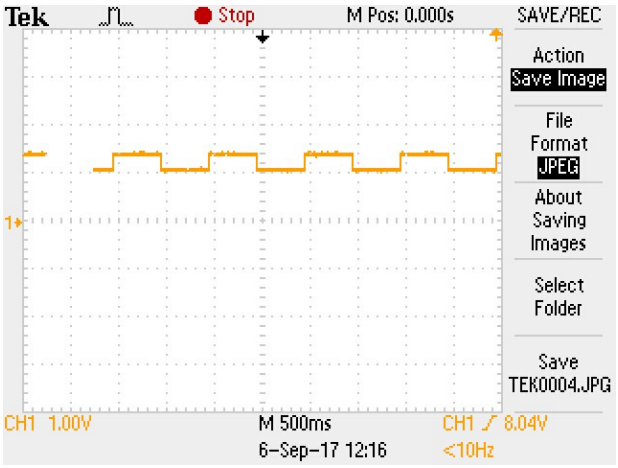

Fig 6 : Voltage level at non-inverting output

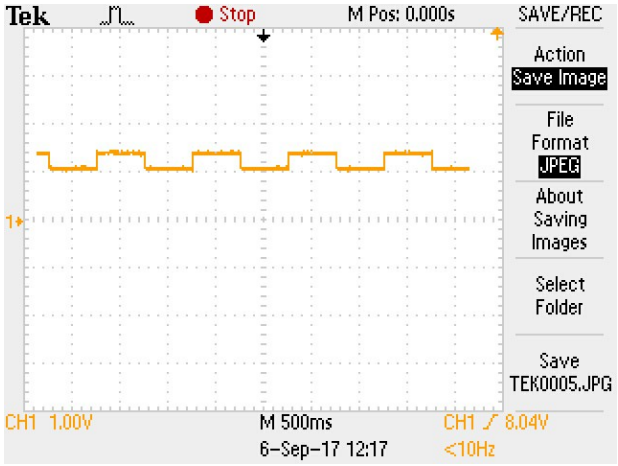

Fig 7 : Voltage level at inverting output

Faulty IC :

ROACH board in OFF condition

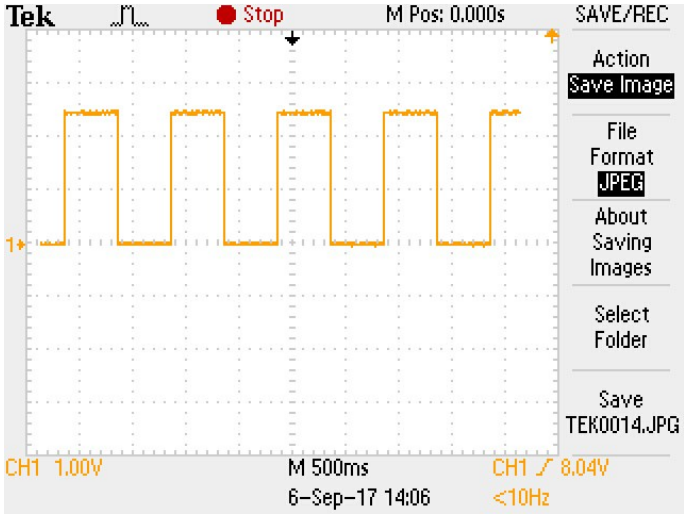

Fig 8 : Voltage level at input

ROACH board in ON condition before programming the FPGA

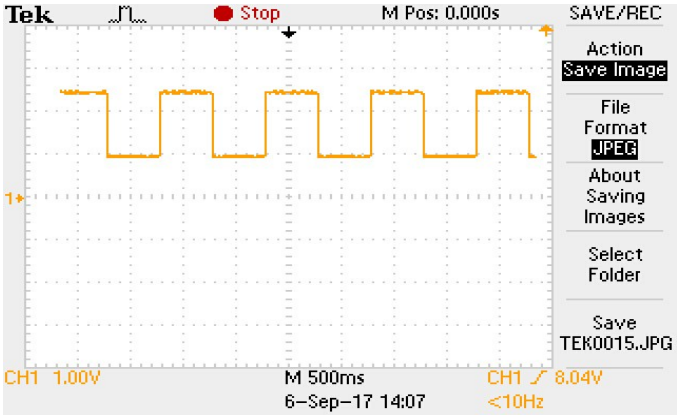

Fig 9 : Voltage level at input

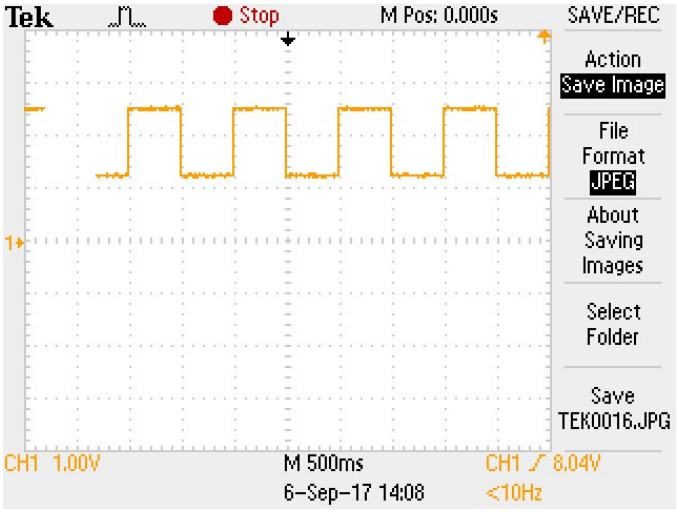

Fig 10 : Voltage level at non-inverting output

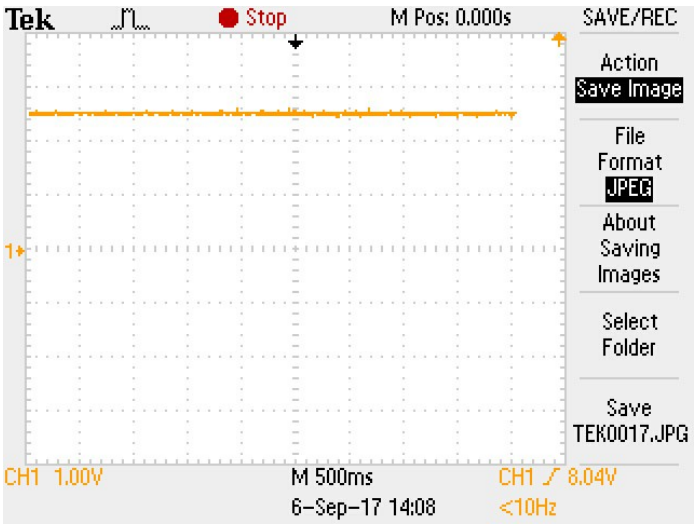

Fig 11 : Voltage level at inverting output

ROACH board in ON condition and after programming the FPGA

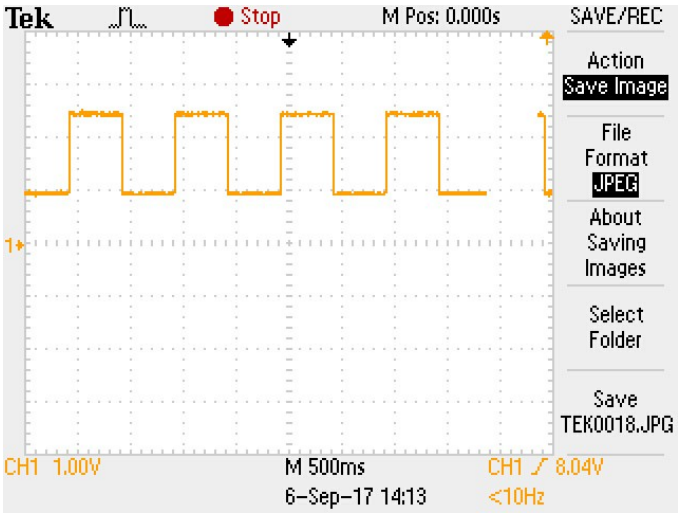

Fig 12 : Voltage level at input

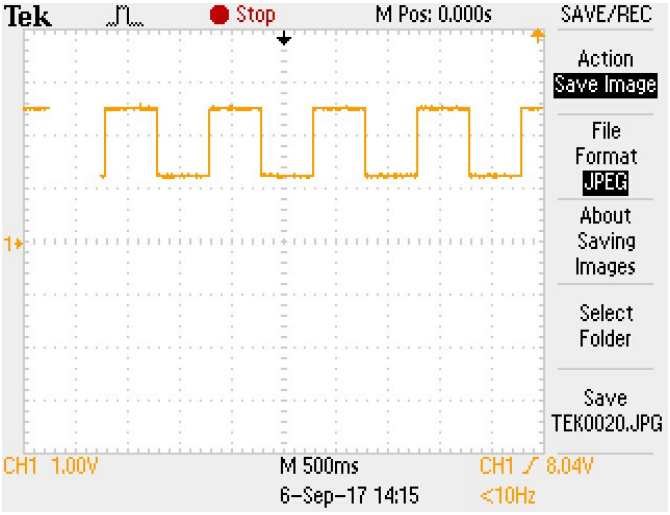

Fig 13 : Voltage level at non-inverting output

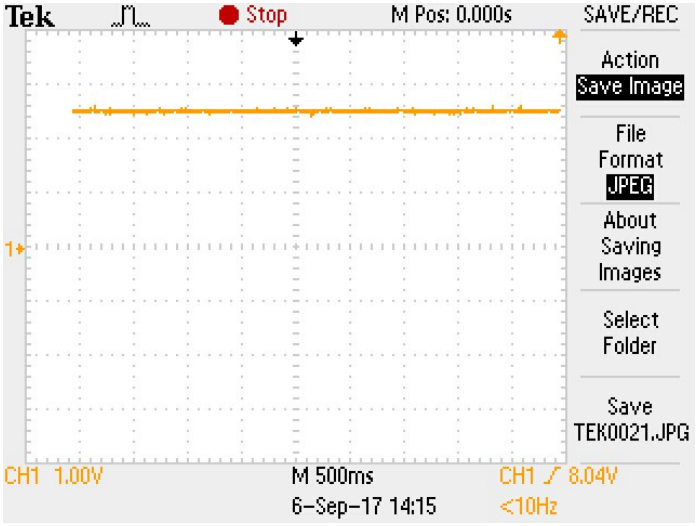

Illustration 1: Fig 14 : Voltage level at inverting output

Conclusion : Problem has been observed at the IC SN65LVDS1 of iADC. Replacing the faulty IC has solved the problem.