

INTERNAL TECHNICAL REPORT

FPGA-based Wideband Beamformer For Focal Plane Array

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Abstract

Surveying and imaging speed of a radio telescope depends on the number of beams forming the field of view and their position with respect to each other. The traditional telescope used either single dipole or horn antenna as a feed system. In FPA dense antenna array with large number of element used as feed system. These elements create multiple beams by collecting the entire electric field in the focal plane.

We describe a prototype design for four elements of focal plane array two beam beamformer. This prototype implemented on ROACH1 (reconfigurable open architecture computing hardware) board using CASPER(collaboration for astronomy signal processing and electronics research). Currently we are working on scalable architecture on ROACH board. This scalable architecture concept first demonstrated for two ROACH boards(eight inputs).

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Chapter 1

Introduction

This project is part of eGMRT proposal. There are three parts in e-GMRT proposal first one is add more antennas in shorter base lines, second one is add more antennas in longer base lines and third one is replace single pixel feed by multi-pixel feed.

Focal Plane Array (FPA) beamformer system was procured from the ASTRON (Netherlands Institute for Radio Astronomy) as a part of 12th plan of expanding the existing GMRT. Focal plane array beamformer system is itself a system generating multiple beams beamformer (Band width= 80MHz) along with this we are implementing our own wide band(Band width=300MHz) and narrowband (band width=25MHz) beamformer.

1.1 Beamforming

Beamforming is a signal processing technique used in sensor arrays for directional signal transmission or reception. Simple beamforming structure base on linear array, where M number of sensor sample the wave field spatially as shown in figure1.2.

The output $y(t)$ at time t is given by an instantaneous linear combination of these samples $X_m(t)$ $m=0,1,2,\dots,M-1$

$$y(t) = \sum_{m=0}^{M-1} [X_m(t)W_m^*] \quad (1.1)$$

where *complex conjugate operation

For example the array response to an impinging complex plane wave $e^{-j\omega t}$ with an angular frequency ω and direction of arrival(DOA) angle θ . Phase at first sensor is zero and phase at M^{th} element is $e^{-j\omega(t-T_m)}$

$$W_d^H(\omega, \theta) = [A_0 \times e^{-j\omega t} A_1 \times e^{-j\omega(t-T_1)} \dots A_{m-1} \times e^{-j\omega(t-T_m)}] \quad (1.2)$$

Weight vector W hold the M complex conjugate weight.

where, A is amplitude for beamshaping and exponential term for beam steering.

1.1.1 Coherent and incoherent Beamforming:

Beamforming is achieved by combining elements in the array in such a way that signals at particular angles experience constructive interference while others experience destructive interference. In beamformer, the antennae signals can be added coherently or incoherently.

Incoherent Beamforming(IA):In incoherent beamformer, the voltage signals (v_i where $i=1,2,\dots,N$) are first converted into power spectra. Then the power signals from the N elements are combined to give the single incoherent beam. As the power spectra of the signals are added, the phase information is lost and no need of phase corrections.[1]

The properties of IA beam output are:

- 1) \sqrt{N} improvement in sensitivity.
- 2) Beamwidth of single antenna.

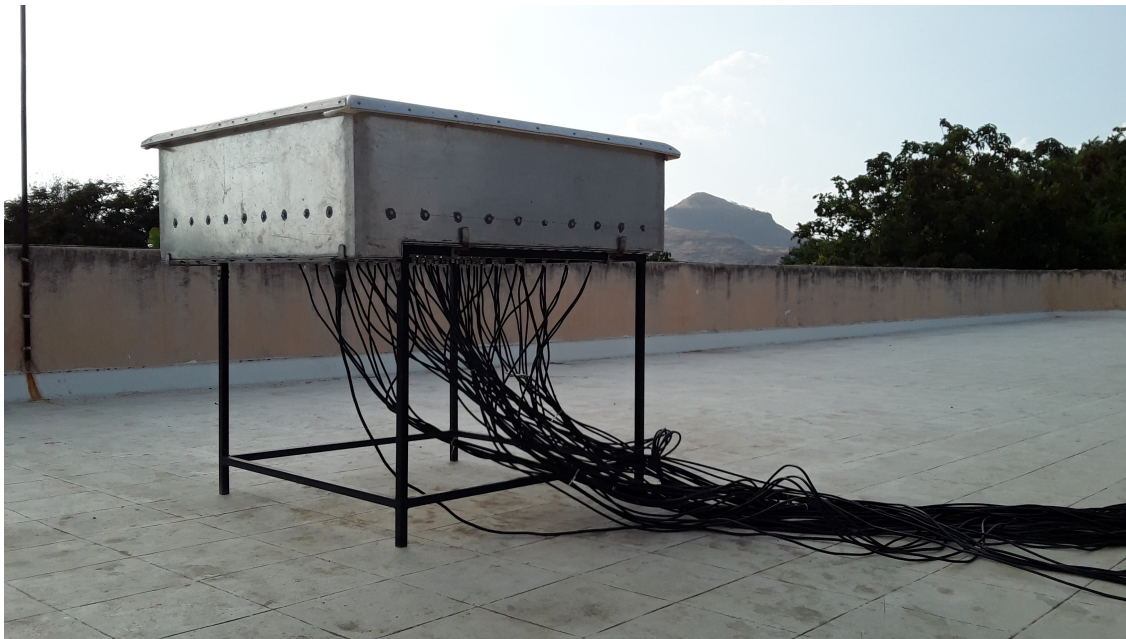


Figure 1.1: Snapshot of the LOFAR FPA feed

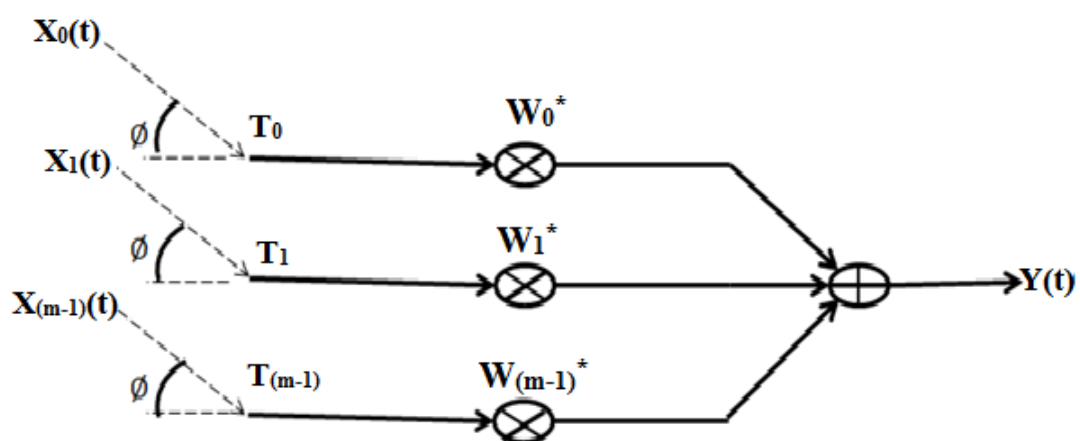


Figure 1.2: Linear array beamformer

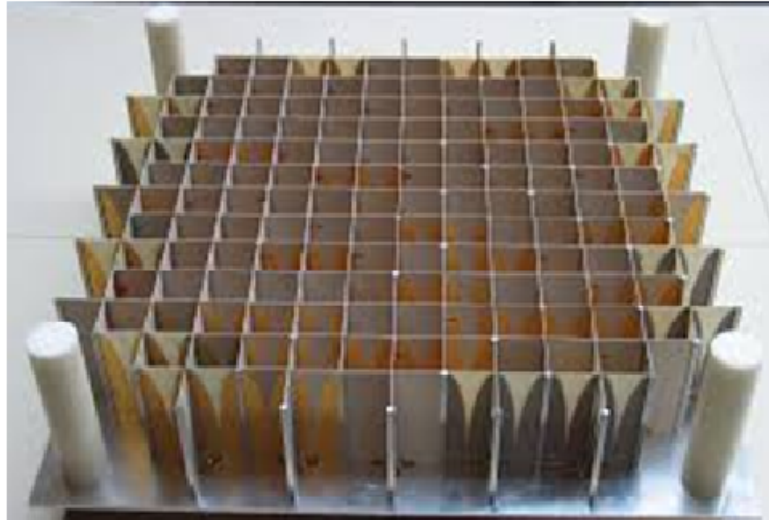


Figure 1.3: Focal plane array feed
[2]

- 3) Application in large scale pulsar search
- 4) The mathematical representation of the incoherent beamformer:

$$B_I = \sum_{i=1}^N V_i^2 \quad (1.3)$$

Coherent beamformer(PA): Voltage signals from the N dishes are combined to give the single coherent beam. As the voltages are added, it should be in phase with each other to get the resultant coherent signal referred as beam.[1]

he properties of PA beam output are:

- 1) N times improvement in sensitivity.
- 2) Beamwidth becomes narrower than the single antenna by nearly 1/N times.
- 3) Application in studies individual known pulsars with its polarimetry studies.
- 4)The mathematical representation of the coherent beamformer

$$B_c = \left\{ \sum_{i=1}^N V_i \right\}^2 \quad (1.4)$$

1.2 Focal Plane Arrays :

Focal plane array is an arrays of sensing elements placed at the focus of a radio telescope.Traditional radio telescopes have only one sensing element at the focus of the telescope, but many of contemporary and upcoming radio telescopes are to be equipped with focal plane arrays.

1.2.1 Advantage of focal plane array feed over single feed:

Improved Antenna Efficiency: The maximum aperture efficiency of a reflector is achieved when the feed matches the focal plane field generated from an incoming plane wave on the reflector.

Field of View (FoV): Discrete FPAs can greatly increase the FoV of an antenna system by placing

multiple beams on the sky but the FoV is not contiguous and to fully sample the sky four or more interleaved pointings are required[3]. Dense FPAs however can fill in these gaps, providing near constant and smoothly varying efficiency and sensitivity across the FoV.

Interference cancellation: The flexibility that beamforming an FPA allows nulls to be established in directions of an interference[4].

Reconfigurability: Dense FPAs lend themselves to electronic beamforming and so offer the flexibility to adapt the element weighting to changing demands and environments. The weighting can be adjusted to balance them for specific purposes. For example in a radio telescope a balance may be selected between maximizing sensitivity and pattern control or interference mitigation and pattern control.

Chapter 2

Hardware and Software

2.1 CASPER

The Center for Astronomy Signal Processing and Electronics Research (CASPER) is a global collaboration dedicated to streamlining and simplifying the design flow of radio astronomy instrumentation by promoting design reuse through the development of platform-independent, open-source hardware and software[5].

The CASPER tool-flow is better known as the MSSGE (Matlab/Simulink/System Generator/EDK) or *bee xps* tool-flow. It is the platform for FPGA-based CASPER development and is the interface between several design and implementation environments. CASPER design environment in GMRT that is used during the course of this project uses following versions of software.

- Matlab R2008a or R2008b (v7.7.0)
- Simulink R2008b (v7.2)
- Xilinx System Generator v10.1.3.1386
- Xilinx EDK v11.5
- Xilinx ISE v11.5
- MSSGE libraries

The aim of the CASPER based designs is to couple the real-time streaming performance of application-specific hardware with the design simplicity of general-purpose software. By providing parameterized, platform independent "gateway" libraries that run on reconfigurable, modular hardware building blocks, we abstract away low-level implementation details and allow astronomers to rapidly design and deploy new instruments. CASPER instruments use reconfigurable open-source hardware built around Xilinx FPGAs. The GMRT uses Virtex-5 SXT95 based standalone FPGA processing board also called ROACH(Reconfigurable Open Architecture Computing Hardware).

The ROACH board also has the following features

- A separate PowerPC runs Linux and is used to control the board
- CX4/XAUI/10GbE Networks Interfacing Cards
- ADC2x1000-8: Dual 8-bit, 1000Msps (or single 8-bit 2000Msps)

Design Flow in MSSGE tool flow

1. Create a Simulink model
2. Compile with BEE XPS.
3. Program your board
4. Test

2.2 ROACH Boards

Reconfigurable Open Architecture Computing Hardware is a standalone FPGA processing board. It is a Virtex5-based upgrade to current CASPER hardware. It merges aspects from the IBOB and BEE2 platforms into a single board.

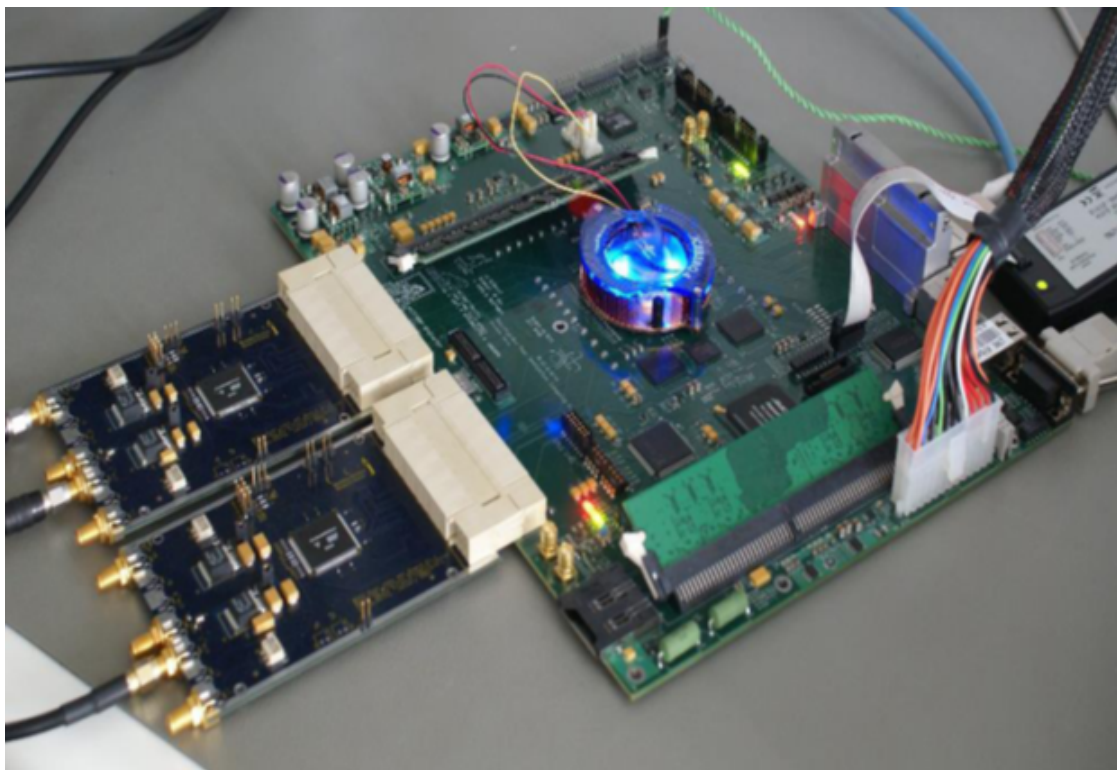


Figure 2.1: Virtex 5 ROACH board

The CX4/XAUI/10GbE interfaces of both are kept, while combining the Z-DOK daughter board interface of the IBOB with the high bandwidth/capacity DRAM memory and standalone usage model of the BEE2. ROACH is a single-FPGA board, dispensing with the on-board inter-FPGA links in favor of 10GbE interfaces for all cross-FPGA communications[5].

Chapter 3

Simulation

Simulations for understanding basic beamforming concepts like beam steering, coherent and incoherent addition and phase correction effect on correlator output were carried out in MATLAB.

3.1 Phase correction using weight multiplication

The effect of phase correction on the cross correlation phase can understand by generating two random sequences $x_1(n)$ and $x_2(n)$ which are beamformer inputs compute 1024 point FFT for this time domain signal and convert it to the frequency domain i.e $X_1(\omega)$ and $X_2(\omega)$.

Compute cross-correlation of two signals using FFT property convolution in time domain is equal to multiplication in frequency domain,

$$x_1(n) * x_2(n) \leftrightarrow X_1(\omega) \cdot X_2(\omega)$$

Then record cross-phases. Multiply these cross-phases to the $X_1(\omega)$, it means we correct the phase for $X_1(\omega)$. Observe cross- phase cancellation at the output of correlator(figure3.1).

3.2 Coherent and incoherent addition

To understand the difference between coherent and incoherent addition we generate two sine waves with same amplitude, first with zero phase and second with 90 degree phase offset. First add two sine waves with same amplitude and zero phase, i.e coherent addition. Then add two signal one with zero phase and another with 90 degree phase offset, i.e incoherent addition. Amplitude ratio between coherent and incoherent addition is 1.414 ($\sqrt{2}$) as shown in figure3.2. Similarly for four signal addition add four signals with one amplitude and zero phase and add four signal first with zero degree phase, second 90degree phase, third 270 degree phase and fourth with 360 degree phase. Amplitude ratio between coherent and incoherent addition is 2(i.e $\sqrt{4}$) as shown in figure3.3. From above two examples ratio between coherent and incoherent addition is \sqrt{N} , N is number of signals get added.

3.3 Beam steering for four elements uniform linear array using pattern multiplication method

The total radiation pattern of an antenna array is the product of the element pattern and the array factor (AF). This is known as a pattern multiplication. The element pattern is dependent on the physical dimensions and EM characteristics of the radiating element. AF depends on the amplitude, phase and position of each element in the array.

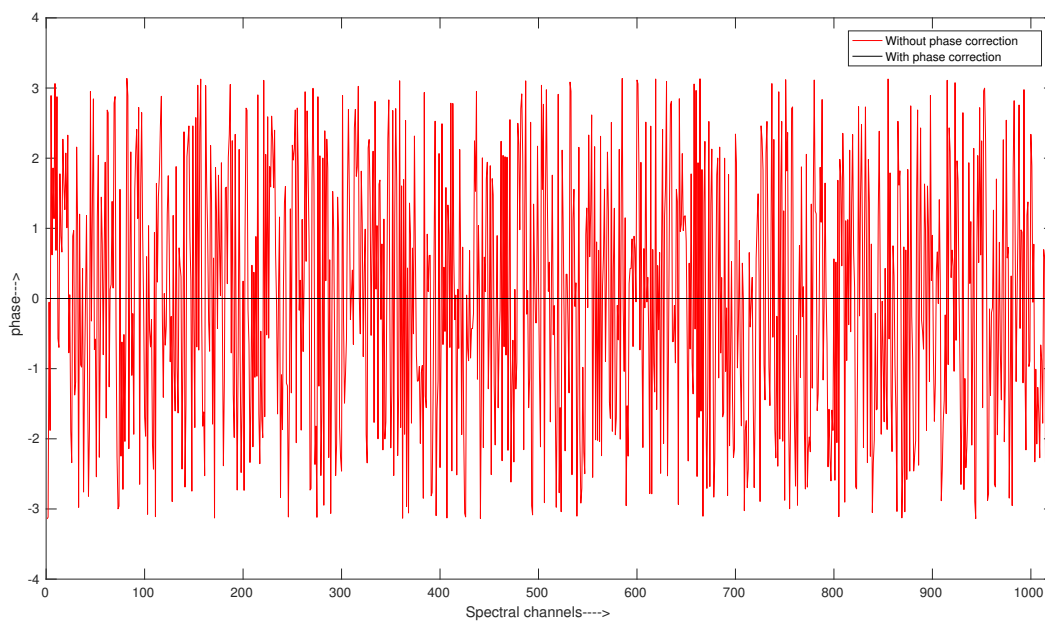


Figure 3.1: cross-correlation phase with phase correction and without phase correction

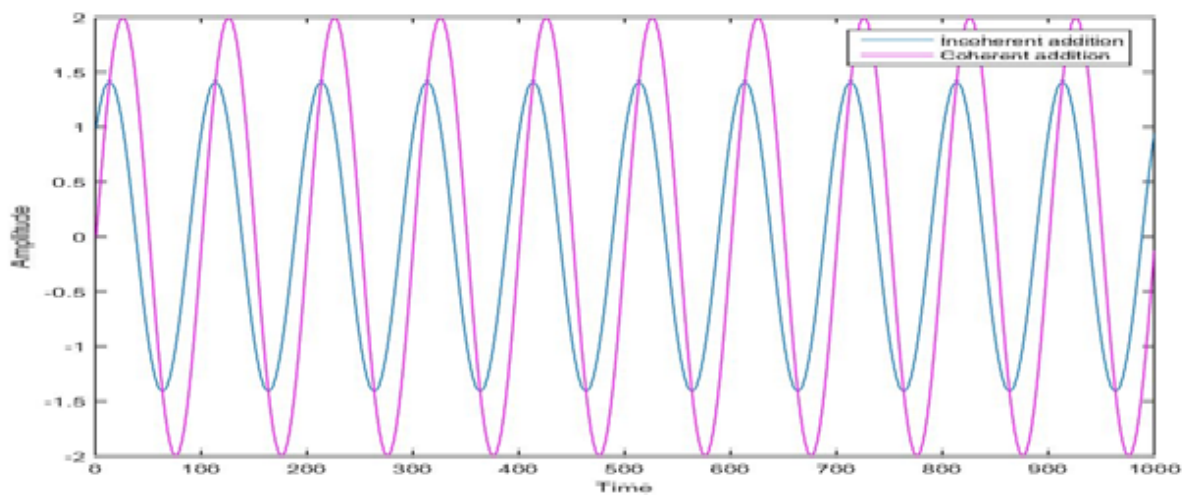


Figure 3.2: Coherent and incoherent addition of two signals

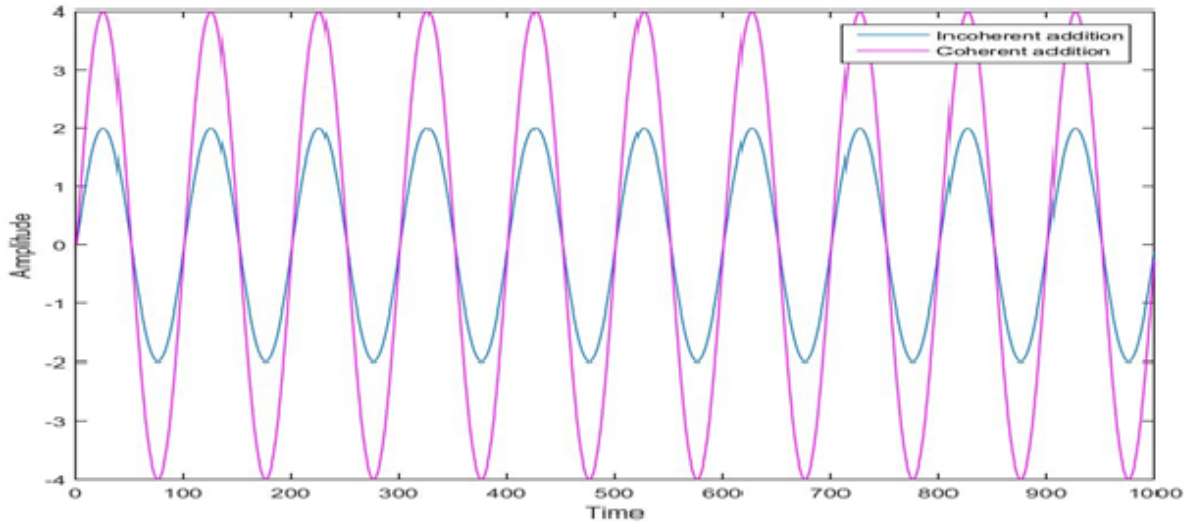


Figure 3.3: Coherent and incoherent addition of four signals

To understand beamsteering concept we simulated four element linear array with $0.5 * \lambda$ element spacing at frequency 1.1GHz using pattern multiplication method. These elements are cosine elements. element pattern= $\cos(\Theta)$

Array factor for linear array is,

$$AF = \frac{\sin((\psi * n/2))}{n * \sin(\psi/2)}$$

where ψ is phase difference.

$$\psi = 2 * \pi / \lambda * d * (\sin(\Theta) + \sin(\phi))$$

A beamsteered linear array is an array where the phase shift $\sin(\phi)$ is a variable thus allowing the main-lobe to be directed toward any direction of interest.

$$\text{Array pattern} = \text{element pattern} * AF$$

Element pattern is $\cos(\Theta)$, therefore element having half power beamwidth is 60degree. We simulated four element array by applying 30,60 and 90 degree ϕ (steering) angle as shown in figure3.4,figure3.5 and figure3.6.

Simulation Results:

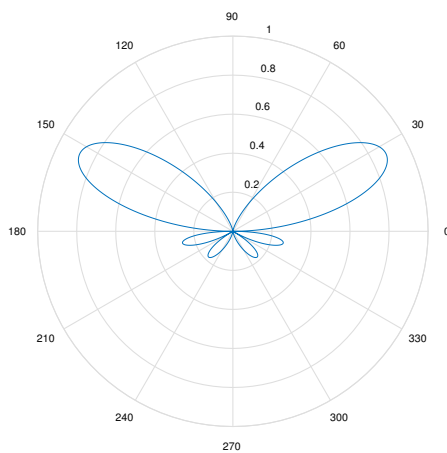


Figure 3.4: Four element simulation using pattern multiplication method at 30 degree steering angle

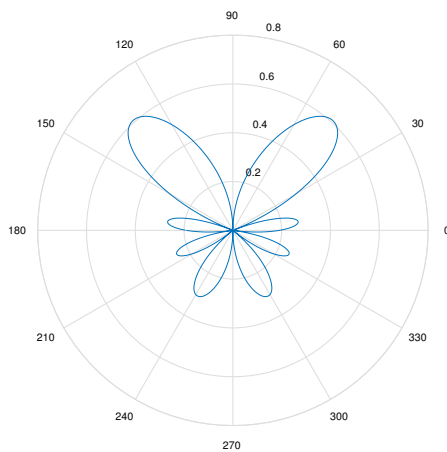


Figure 3.5: Four element simulation using pattern multiplication method at 60 degree steering angle

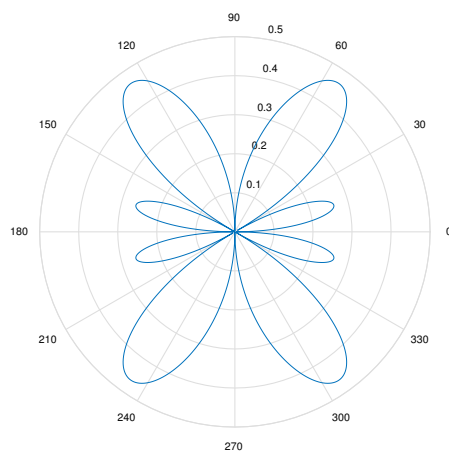


Figure 3.6: Four element simulation using pattern multiplication method at 90 degree steering angle

Chapter 4

Single-Board Beamformer

4.1 Four-antenna two-beam coherent beamformer specifications

Bandwidth:300MHz
Number of beams:2
FFT size =512 points
Spectral channels:256
Number of antennas :4
Polarization :1

4.2 FPA beamformer design block diagram

ADC:The ADCs interfaced to the ROACH board are ADC2x1000-8. They have operated at 600MHz and give an 8 bit digital output through 4 channels each operating at 150MHz.

PFB: The polyphase filter bank implements a hamming window.The PFB is used to reduce spectral leakage and to increase signal to noise ratio. The data rate at the output will be 4 channels each of 18 bits at 150MHz.

FFT:The FFT block used is FFT Bipler Real 4x (real-sampled bipler FFT). This block computes the real-sampled Fast Fourier Transform using the bipler FFT algorithm to transform two real streams. The data rate of operation at the FFT output is 36 bits each at 300MHz. One of the streams gives even channels while the other gives odd channels. Each channel consists of an 18 bit real part and an 18 bit imaginary part. The channel itself is 36 bits with 17 bits after the binary point. This can be best explained from the figure4.2.

Weight multiplication: Proposed system design forms multiple beams along different directions by multiplying appropriate weight values to the antenna signals. Weights are in the form of phase and amplitude using look up table it converted in to the complex number. Output of look-up table in the form of complex number it multiply with unsigned 3 bit amplitude output of this multiplier is complex weight. Multiplication of FFT output and complex weights which is also complex number performs using each channel complex multiplier as shown in figure4.3. Weight multiplication block output is 18 bit real part and an 18 bit imaginary data for each channel. The channel itself is 36 bits with 17 bit binary point.

Equalizer block:This block scale down the amplitude by a given factor to avoid the over flow during correlation and integration. The scaling factor depends on the power level of the signal. This block casts the 36 bits input data into 8 bits data.

Correlation and Integration block: The correlator block in the design performs the product of voltages of two channels. The output of the equalizer is 8 bits. This is fed to an accumulator which gives a 32 bit output.The typical integration time is in second. But it can vary in accordance of data rate and noise level. The output is all the auto-correlated and the cross-correlated pairs. This correlated data is transferred into shared BRAM so that host PC can read correlated data and store it on a disk for further use.

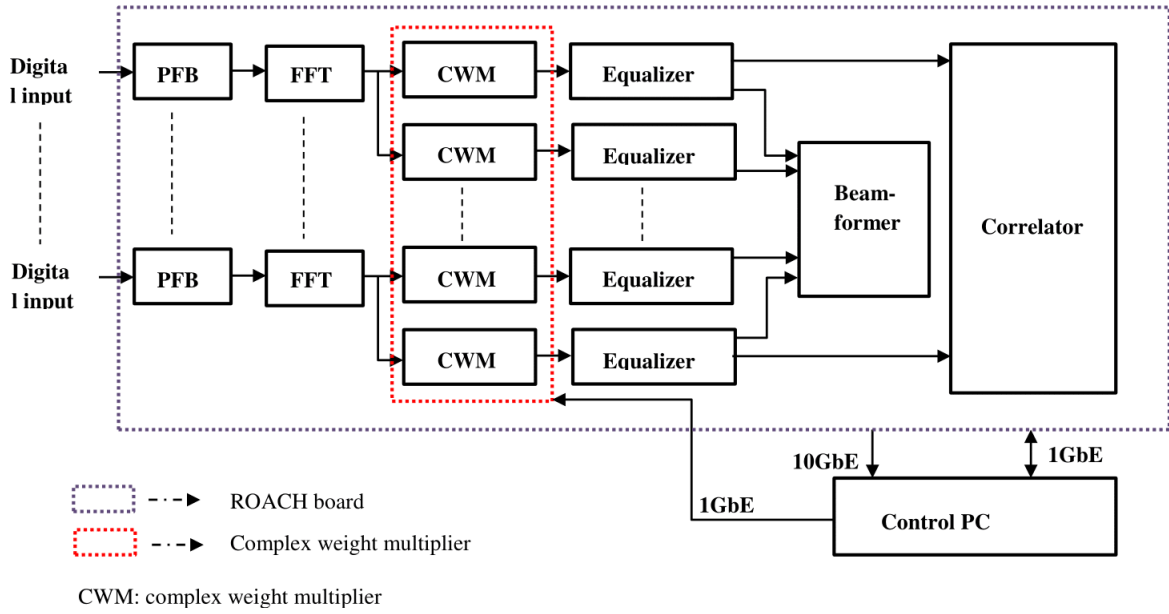


Figure 4.1: Block diagram of Multi-channels Beamforming for Focal Plane Array

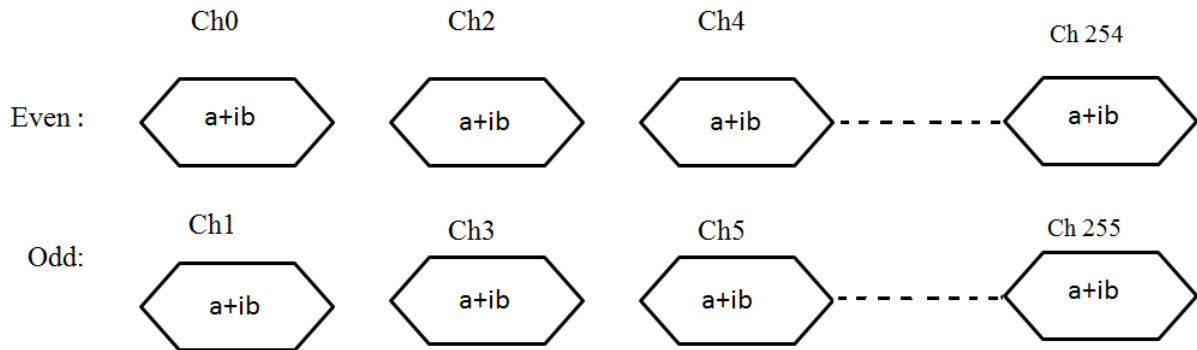


Figure 4.2: FFT Channel Output

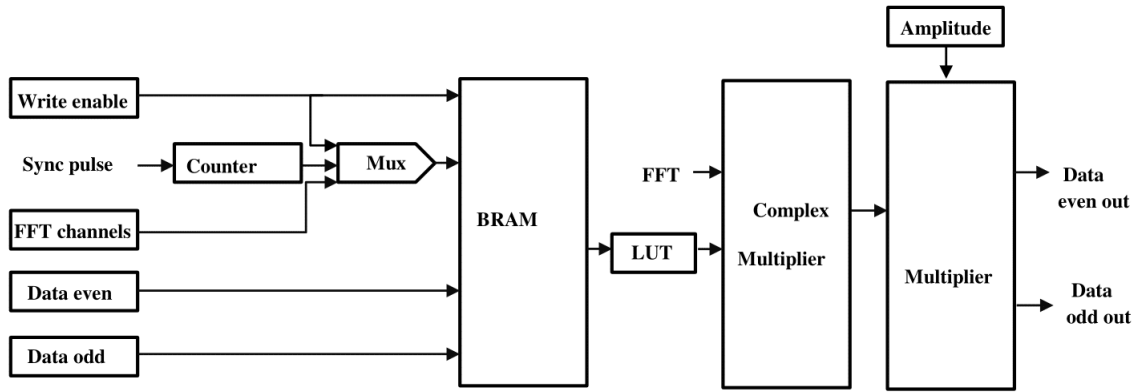


Figure 4.3: Weight multiplication block

Beamforming: Coherent beam forming is the adding and squaring of voltages from two or more input signals. In this case, only the addition of antenna signals is carried out on FPGA. Post-processing like squaring done in software, due to this complex addition optimum hardware resource utilization possible.

4.3 Phase multiplication subsystem

Proposed system design form multiple beam along different direction by multiplying appropriate weight values to the antenna signals.

The data is coming in two parallel FFT channels i.e. Even and odd Channel. So, two BRAMs are used to store the phase values for Even and odd respectively, whose depth is half the number of spectral channels(256). These BRAMs will store the phase values for even and odd channels separately which are written in these memory during run time and read the phase value and multiply to each channel. So for the switching this logic in two modes back and forth, a two input multiplexer used for selecting the address line and write enable signal is select control for this multiplexer. When write enable is high, the address line that drives both BRAMs is coming from external peripheral (python script running on host PC) and both the BRAMs are in writing mode. Now we start sending the data to BRAM and incrementing the address values accordingly. When the writing operation is over, write enable goes low and mux will switch the address lines.

The address comes from a counter. The number of bits is $\text{FFT channel}/2$. This counter runs synchronously with the whole design that means the counter output (address) is always equal to channel numbers of data values coming for phase correction.

Following are the parameters for the BRAM used :

a. sync_pulse (reset counter enabled by sync) and `fft_channel` (`fft0`) are used for addressing the BRAMs. They are multiplexed (Mux) as shown in the figure4.3. `fft_channel` is written through a python script.

b. write enable enables the write modes of the BRAM and used as a select line for the addressing multiplexer.

c. data even and data odd are the Phase Even and Odd values respectively which are written through software registers using the python scripts.

Complex weight contain phase as well as amplitude. Output of complex multiplier is phase multiplied signal, amplitude multiplication perform using simple multiplier block as shown in figure4.4.

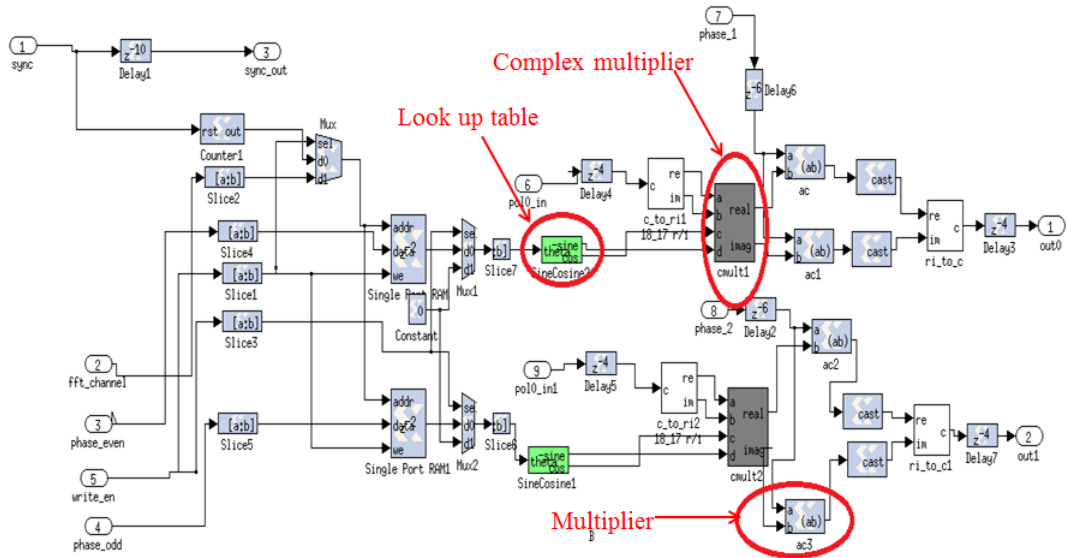


Figure 4.4: Weight multiplication block snap shot

4.4 Coherent sum subsystem

The Coherent Beamforming logic equals the Square of Sum of Antenna voltages. Hence, its mathematical representation is as shown in figure 4.5:

$$\text{Coherent sum} = (V_1 + V_2 + V_3 + V_4)$$

Where V_1, V_2, V_3 and V_4 are FFT of voltages from antenna one, two, three and four respectively. Output of coherent sum subsystem is complex values of antenna signals, for example $V_1 = (a_1 + jb_1), V_2 = (a_2 + jb_2), V_3 = (a_3 + jb_3)$ and $V_4 = (a_4 + jb_4)$ are antenna signals.

$$\text{Real part of coherent sum} = (a_1 + a_2 + a_3 + a_4)$$

$$\text{Imaginary part of coherent sum} = (b_1 + b_2 + b_3 + b_4)$$

Send complex addition of voltages through 10GbE link to the control PC. Post-processing like squaring done in software, due to this complex addition optimum hardware resource utilization possible.

4.5 UDP packet format design and 10GbE packetization

The packetized design for the 10GbE is a fairly complex system. This section will briefly describe the design. The data is concatenated before packetization in the form of real and imaginary part with 16 bits each and other 32 bits padded with zero resulting in 64 bits entity. The main block responsible for the packaging of the data is the FIFO. In FIFO acts as a memory buffer which can read and write simultaneously. It works such that one 64 bit data is written in one clock and is read in the next clock. For the two different concatenated packages two different FIFOs are used. The 2nd FIFO is delayed by 128 clocks to increase the package depth by 128bytes. This results in the packet configuration as seen in Figure 4.6.

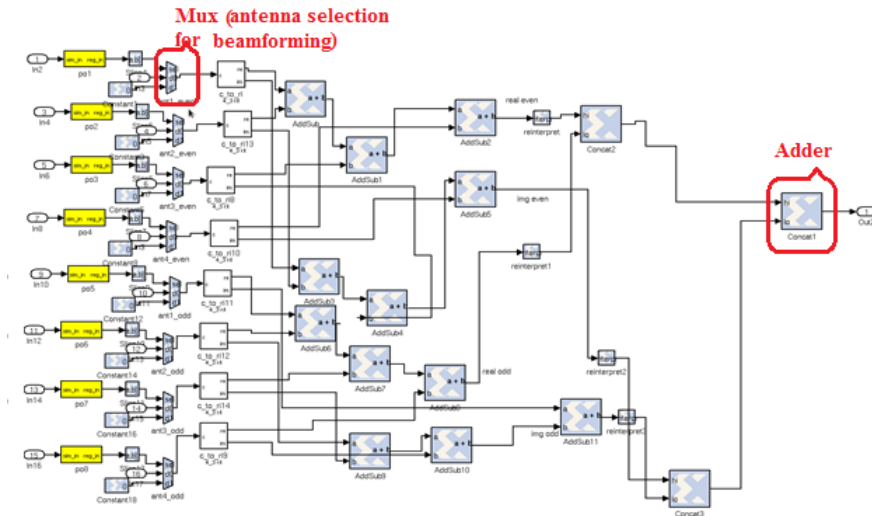


Figure 4.5: Coherent sum snapshot

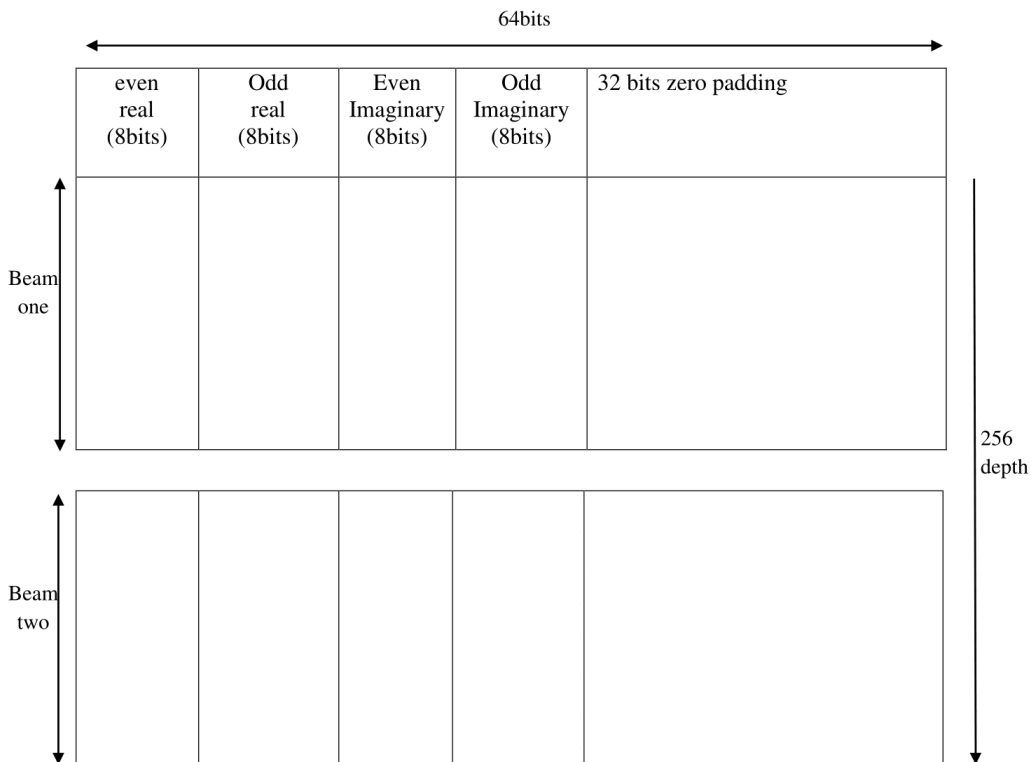


Figure 4.6: UDP Packet format

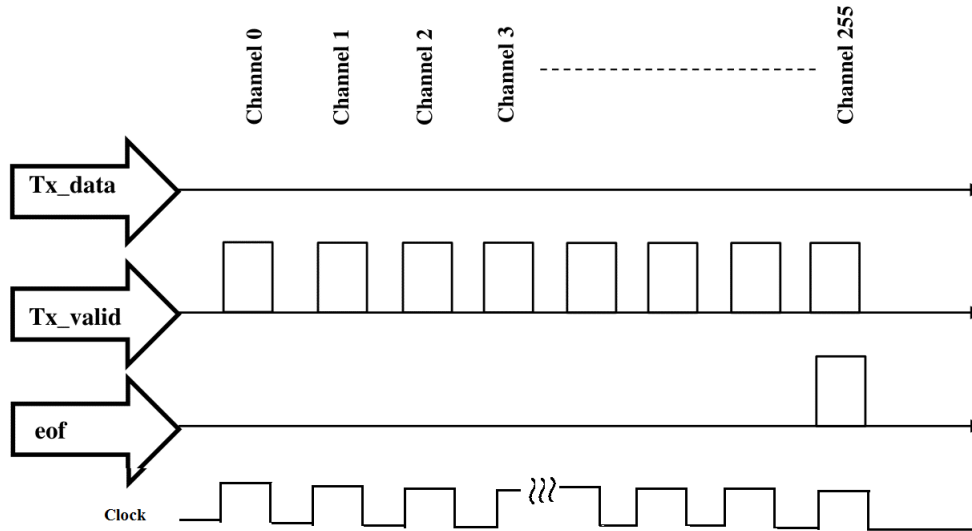


Figure 4.7: Valid signals in 10GbE

4.5.1 10GbE packetization

The 10GbE block requires inputs as tx_data, tx_valid, eof, reset_gbe, tx_destination_ip and tx_destination_port. Out of these eof, tx_valid and tx_data signals as shown in figure4.7 are generated inside the subsystem after coherent sum. For reset_gbe, tx_destination_ip and tx_destination_port, software registers are added to the design. These software registers are configured using python script.

The figure4.8 shows the 10GbE setup within the design. The 10GbE block used is the ten_GbE_v2 block from the BEE_XPS System Block set in the Simulink library.

4.6 Post processing and Depacketization

4.6.1 Packet Capturing

The standard packet analyzer tool, Wireshark, has been used to verify the transfer of packets. This software gives valuable information such as rate of data transfer per packet, packet size along with various other attributes of the packet as it passes along the network. However, the actual utility for packet capture is GULP. This is an open source software which can read directly from the network interface and write to disk. The packet capturing capability of GULP is dependent on the data rate.

4.6.2 Depacketization

Depacketisation is the process of de-segmenting the packet in order to make it compatible for further processing. This is done by a basic 'C' programming. A packet of size 2048 bytes is split into 2 packets of size 1024 bytes each. The data packet is separated in to real and imaginary values. At the output of depacketization, we get real and imaginary files for each beam.

4.6.3 Post Processing

In post processing, the data received from beamformer i.e. four text files example real_beam1.txt, img_beam1.txt, real_beam2 and img_beam2.txt. These files contain coherent sum of antenna signals $(V_1 + V_2 + V_3 + V_4)$, we obtain intensity from coherent sum by squaring this coherent sum output, i.e. $(V_1 + V_2 + V_3 + V_4)^2$.

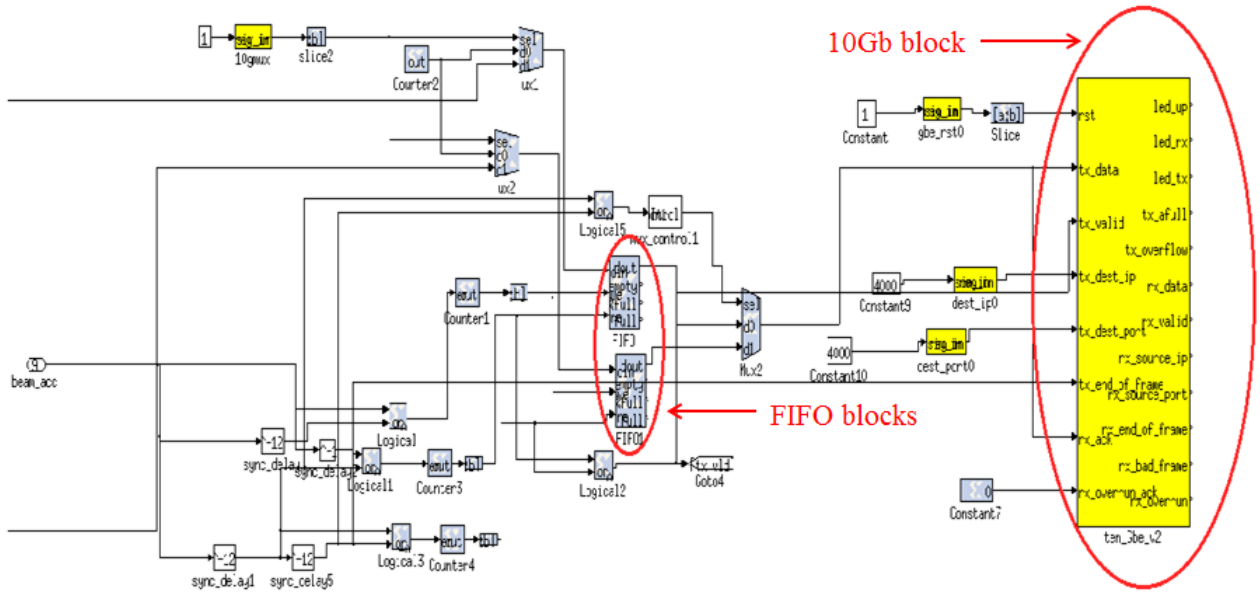


Figure 4.8: 10GbE Block in the Simulink Library

$V_1 = a_1 + jb_1, V_2 = a_2 + jb_2, V_3 = a_3 + jb_3$ and $V_4 = a_4 + jb_4$ these are signals from antenna one, two, three and four respectively. Then coherent sum of this antenna signal is complex number which contain real part $(a_1 + a_2 + a_3 + a_4)$ and imaginary part $(b_1 + b_2 + b_3 + b_4)$. From this real and imaginary part we get intensity.

Chapter 5

Scalable Architecture

To increase number of inputs we introduce the concept of scalable architecture. We increase number of inputs by adding ROACH boards. First we demonstrate with two boards(8 inputs).

5.1 Specifications

Bandwidth: 300MHz
FFT size =512 point
Spectral channels=256
Number of antennas =8
Polarization =1
UDP packet size=2090Bytes
Correlation: offline
Number of beams =2

5.2 Block diagram

The coherent sum from each ROACH board (locked to the sync) is send to a control machine. The overall addition happen on this machine. Regarding correlation, the data must be available from each board to get at least one unique cross product with each antenna. For this purpose, we bring the spectral data of each antenna and carry out an offline correlation and accumulation in the control machine. The data come in the same 10GbE packet as the coherent sum. We do not need a real-time correlator working with the beamformer, therefore we perform offline correlation in control machine. Once the weights are calculated and loaded, the correlator mode is not needed. This eliminates need for developing a "ring" type architecture as shown in figure5.1 where the data from each board goes to the other for computing the cross products.

5.3 Weight multiplication

In this architecture for beam shaping and steering we apply complex weights. Complex weights contain phase and amplitude. This section contain weights multiply element wise as well as channel-wise therefore we add one more BRAM to amplitude channel-wise multiplication as shown in figure5.2 other part of subsystem is same as single board weights multiplication subsystem.

5.4 Packetization

The packetized design for the 10GbE is a fairly complex system. In this part we can select correlatore or beamdata at the output of 10GbE. The data is concatenated before packetisation in the form of real

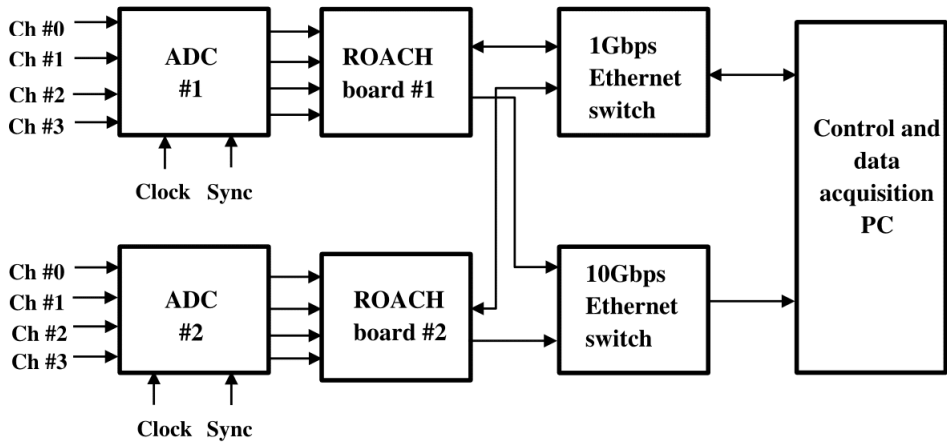


Figure 5.1: Scalable architecture block diagram

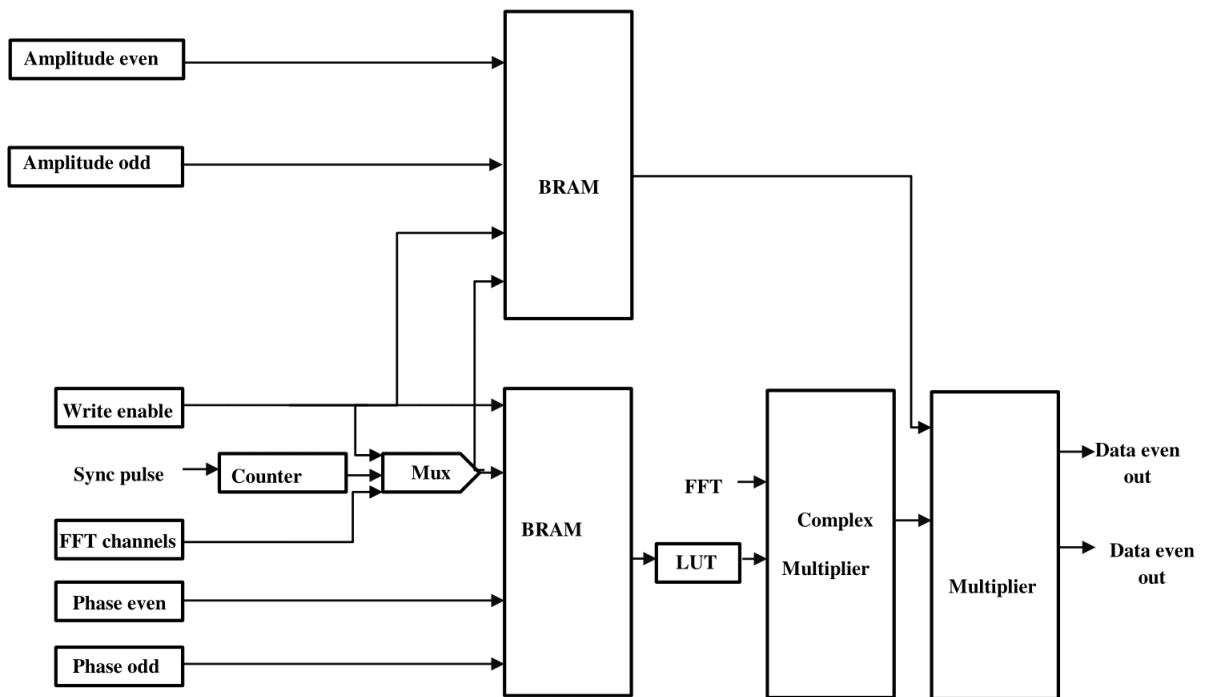


Figure 5.2: Scalable architecture weight multiplication block diagram

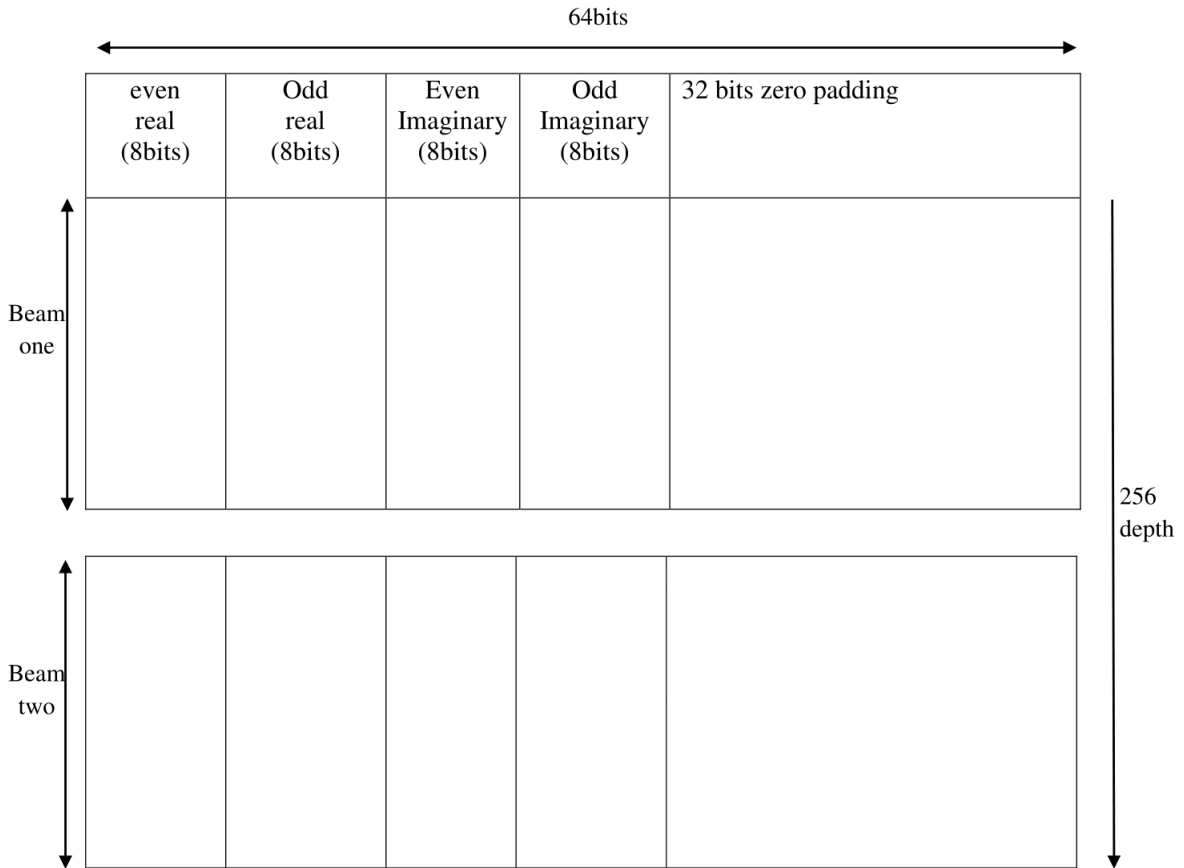


Figure 5.3: Beam-data UDP packet structure

and imaginary part of 16 bits each and a other 32 bits padded with zero resulting in 64 bit entity for beamformer and for correlator concatenated in the form of antenna1 antenna2 antenna3 and antenna4. The main block responsible for packaging the data is the FIFO. In the most basic sense the FIFO acts as a memory buffer which can read and write simultaneously. It works such that one 64 bit package is written in one clock and is read in the next clock. For the two different, concatenated packages two different FIFOs are used. The 2nd FIFO is delayed by 128 clocks to increase the package depth by 128bytes. This results in the packet configuration as seen in Figure5.3 for beam data and Figure5.4 for correlator data.

5.5 Depacketization and post processing

In this architecture we perform offline correlation. Beam as well as correlator output is obtained through 10GbE port so depacketization contains two parts one for beam data depacketization and other for correlator data depacketization.

Depacketization of beam data Packets obtained from the different boards are separated according to their destination IP. A packet of size 2048 bytes is split into two parts of size 1024 bytes. This part is again separated into two subparts: real and imaginary. At the output of depacketization, we get real and imaginary files for each beam for each roach board. Two boards (eight inputs) beamformer obtain eight files.

Depacketization of correlator data Packets obtained from different boards are separated according to their destination IP. A packet of size 2048 bytes is split into two segments of size 1024 bytes. The first segment is again separated into four subsegments, i.e. real part of input one, real part of input two, real part of input three, and real part of input four. The second segment is separated into four sub-segments, i.e. imaginary part of input one,

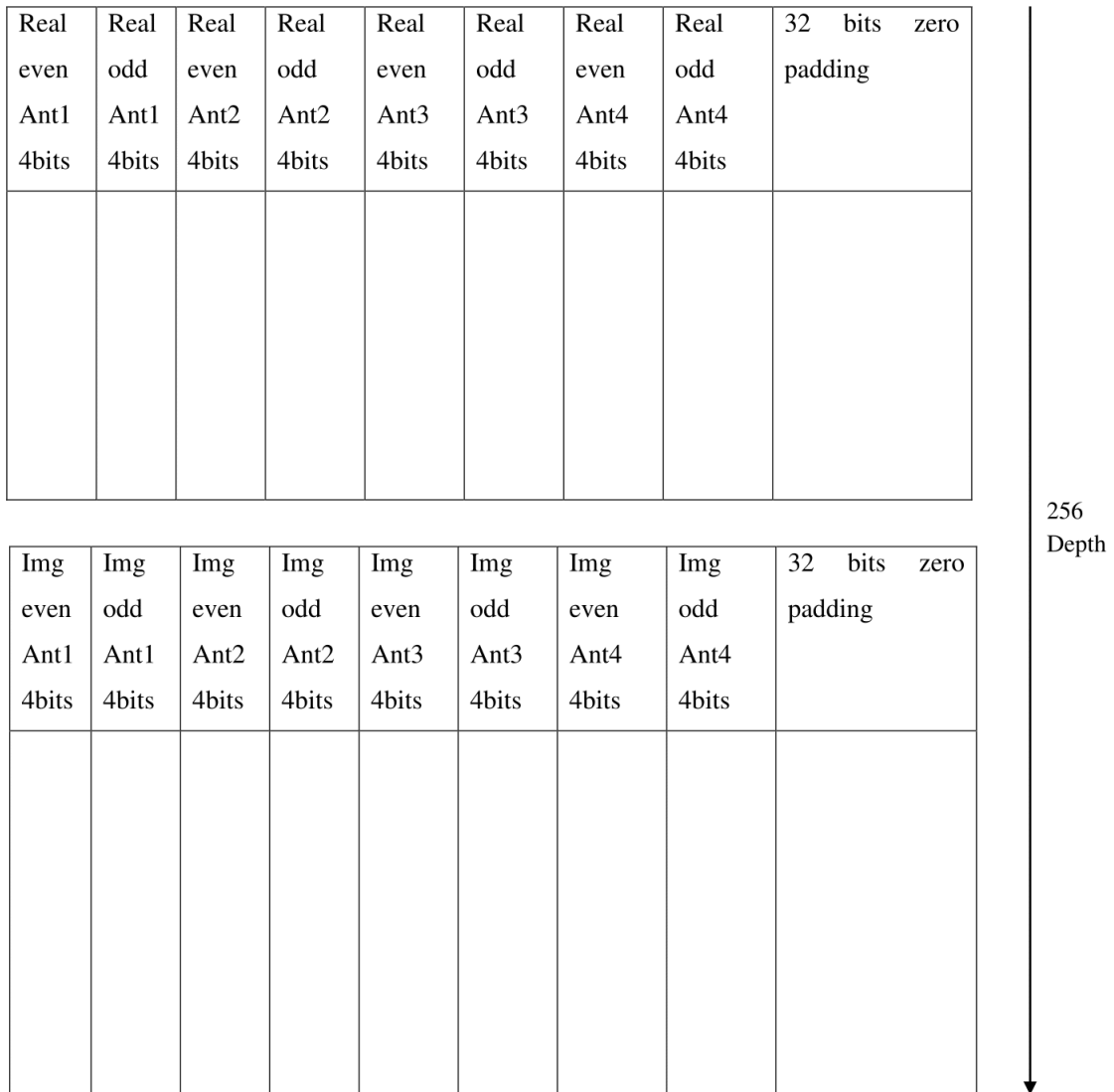


Figure 5.4: correlator-data UDP packet structure

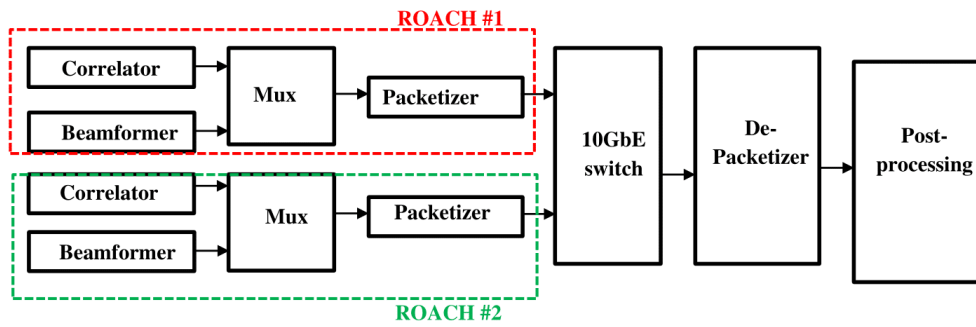


Figure 5.5: Data flow

imaginary part of input two, imaginary part of input three and imaginary part of four.

5.6 Data flow

Mux: Correlator output is not needed frequently, use mux select between correlator and beamformer data due to this FPGA resource utilization is less as shown in figure5.5.

Packetizer: Beam or correlator data transmitted through packetizer in the form of UDP packets.

10GbE switch: Packets coming from different ROACH board pass through 10GbE switch to the control machine.

Depacketization: By running 'C' program the control machine, de-packetize the beam or correlator data.

Post-processing: After depacketization depending of selected mode we get coherent sum as an output or FFT of voltage signal. Using MATLAB correlation script we can compute cross phase between signal and beam output.

Chapter 6

Resource Utilization

6.1 ROACH-1 design resource utilization:

Four inputs (single ROACH board) design and scalable architecture (two-board design) are design and implemented in ROACH one environment. According to the number of beams resource utilization analyzed as shown in figure 6.1.

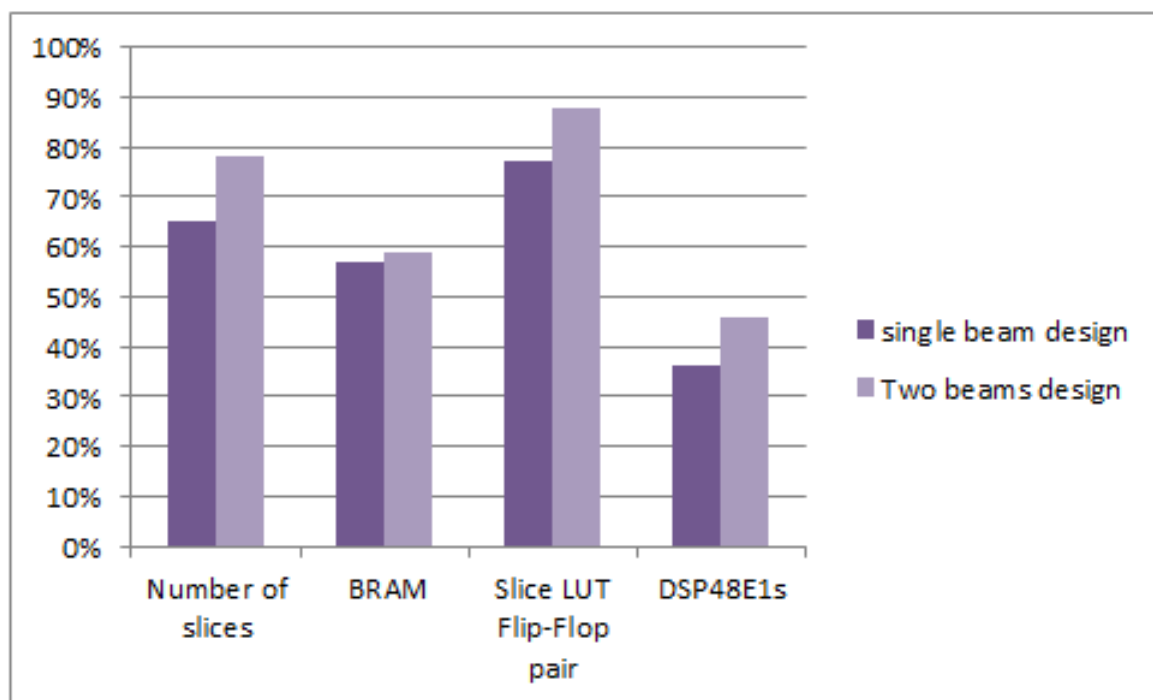


Figure 6.1: Resource estimation for ROACH-1 designs

6.2 ROACH-2 designs

ROACH-2 is advance version of ROACH-1. It contains vertex-6 FPGA .This FPGA contain large number of resource as compared to vertex-5. We compiled varies designs by varying number of beams as shown in figure 6.2. In ROACH-1 board we can form maximum two beam with 256 spectral channels. With ROACH-2 board we compiled up to four beam with 256 spectral channels.

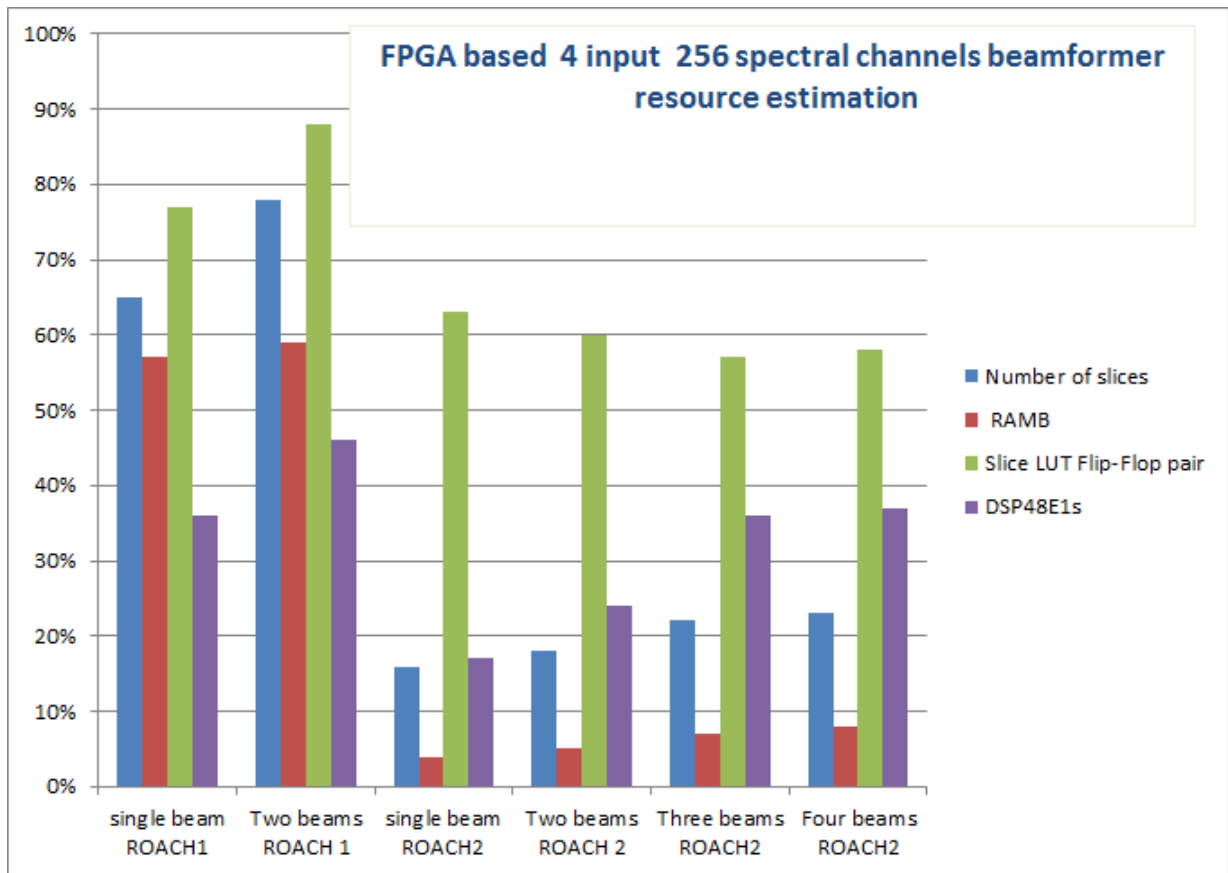


Figure 6.2: Resource estimation for ROACH-1 design

Chapter 7

Experimental Setup

7.1 Lab Test setup

System level design of the setup:

From the figure7.1 the following details must be noted:

The power input levels from the analog backend or baseband systems are typically -12 to -14 dBm.

The ADC clock frequency is 400 MHz

100Mbps/1Gbps Ethernet cable is used to communicate with the PowerPC

10Gpbs link is used for high speed data transfer (faster integration)

7.2 FPA setup

From the figure7.2 the following details must be noted:

8 × 9 focal plane array feed operated at 1.1 to 1.7GHz

DCU convert RF signal in to base band signal(0-240MHz)[7].

The ADC clock frequency is 400 MHz

100Mbps/1Gbps Ethernet cable is used to communicate with the FPGA

10Gpbs link is used for high speed data transfer (lesser integration)

Steps:1)Radiate -5dBm tone signal at 1.1GHz

2)mesure power at the input of DCU i.e -35 dBm

3)set local oscillater

LO1=3.6GHz at 17dBm

LO2=2.65GHz at 17dBm

4)Mesure output power of DCU at 150MHz

5)Apply this DCU output signal(Base Band signal)to the FPGA-based beamformer

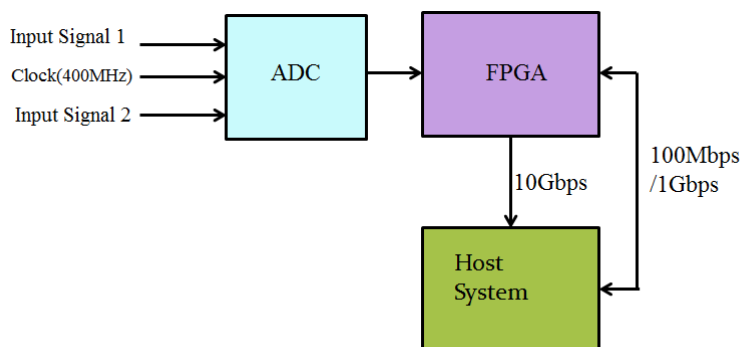


Figure 7.1: Experimental Setup

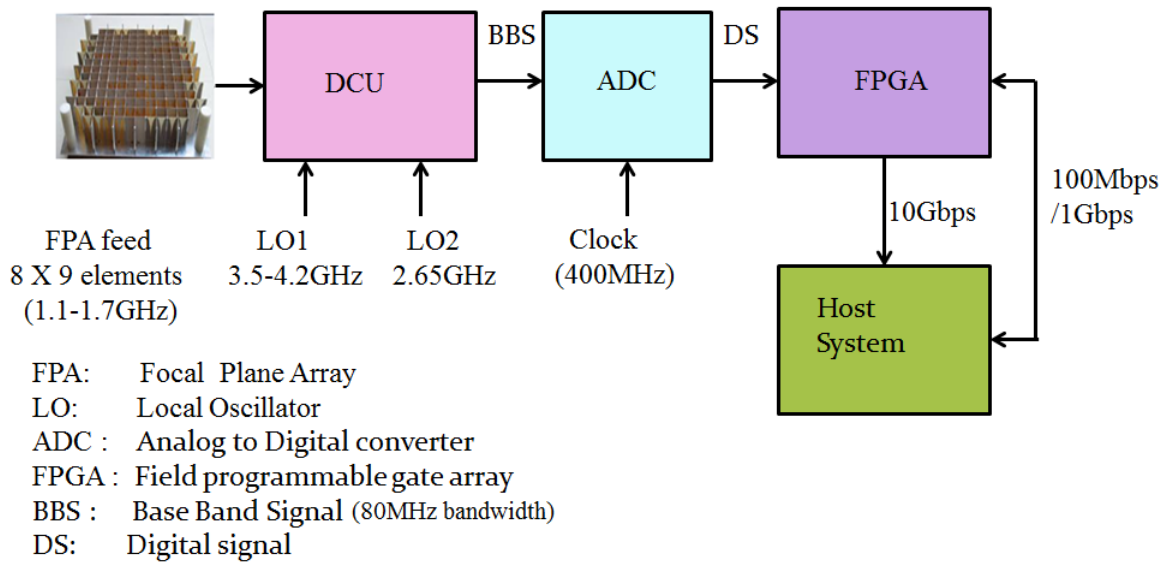


Figure 7.2: FPA test setup

7.3 Scalable architecture test setup

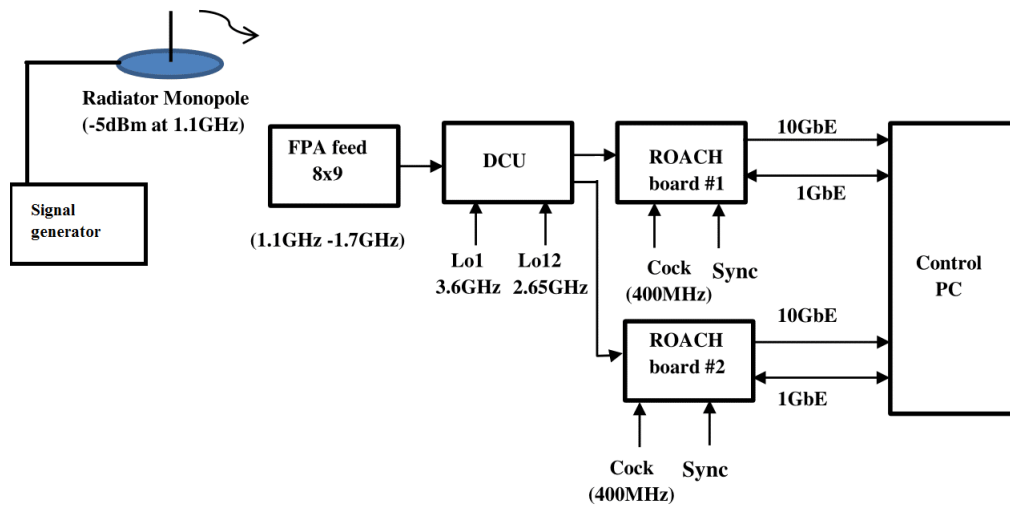


Figure 7.3: Scalable architecture test setup

From the figure 7.3 the following details must be noted:
 8 × 9 focal plane array feed operated at 1.1 to 1.7GHz
 DCU convert RF signal in to base band signal(0-240MHz)[7].
 The ADC clock frequency is at 400 MHz
 100Mbps/1Gbps Ethernet cable is used to communicate with the FPGA
 10Gbps link is used for high speed data transfer (faster integration)
 Sync signal for ROACH boards synchronization i.e 1PPS.
Steps: 1) Radiate -5dBm tone signal at 1.1GHz

- 2)measure power at the input of DCU i.e -35 dBm
- 3)set local oscillator
LO1=3.6GHz at 17dBm
LO2=2.65GHz at 17dBm
- 4)Measure output power of DCU at 150MHz

7.4 Test range for FPA radiation test

To test design with radiation, test range is as shown in figure7.4. It is necessary to place radiating antenna at far field, where the wavefront is planer.

$$\text{Far field distance} = 2D^2/\lambda$$

where,D is dimension of FPA is 1.442m.
 λ is wavelength of FPA is (c/f) 0.2141cm, whit central frequency 1.4GHz
 Therefore far field distance is 19.4m.

To avoid ground reflections place antenna(radiating and Focal Plane Array) at 1.5m above ground.

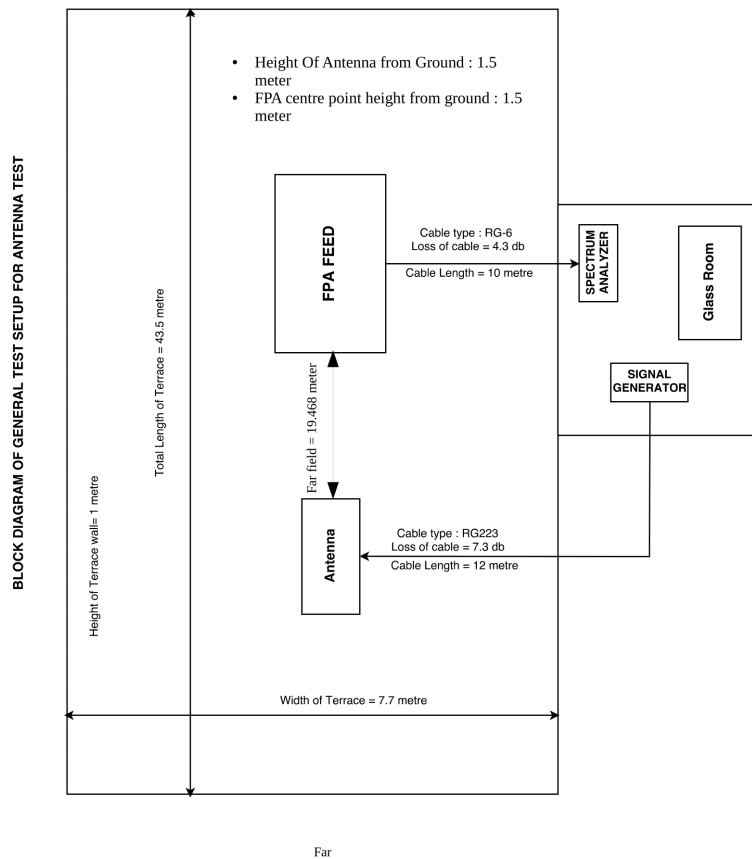


Figure 7.4: Test range for FPA radiation test

Chapter 8

Results And Analysis

Four-antenna, two-beam FPA beamformer design first tested in lab using noise source and sine wave as an input. Further tested it with GMRT antenna signals(single antenna two polarization) and FPA setup. Data obtain from beamformer analyzed using MATLAB code.

8.1 Lab Tests

8.1.1 Case1:Check phase multiplication part by applying sine waves one in phase and another out off phase as an input

Description:Apply sine wave of 100MHz -17dBm power level as an input. First signal multiplied with zero phase and another with 180 degree phase using python script. Record beam data(nearly 100 UDP packets). Beamformer output contain beam one data and beam two data.

Result Analysis:Beam one and two contain coherent sum real and imaginary part of coherent sum. Beam data is coherent sum of in phase and outoff phase sine wave. Therefore wave cancelation observe in beam at 180 degree and -180 degree phase and maximum power at zero degree phase as shown in figure8.1.

8.1.2 Case2:Analyze the effect of different phases on the beamformer output

Description: Apply sine wave at 100MHz -17dBm power level as an input. To one of the input signals multiply different phase values in steps of 10 degree in the range of -180 to 180 degree. At each stage, record beam data.

Result: Analysis: Analyze the effect of phase on intensity. Plot intensity at every phase value. At phase -180 and 180 degree observe zero power due to the addition of two sine waves which are out of phase. At zero degree phase two sine waves add in phase therefore, we get maximum amplitude as shown in figure8.2.

8.1.3 Case3:Analyze effect of phase multiplication on correlator output

Description:Used noise source as an input to the design. Frist measure the phase difference between signals and correct it by applying the difference vale to one of the input. Then record correlator data. Then apply -120,120,180 and -180 degree phases to the one input and kept other input at zero degree phase. Record correlator data at every step and plot it refer figure8.3, figure8.4, figure8.5, figure8.6 and figure8.7.

Results: Analysis:Observe cross correlation phase variation with input signal phase multiplication.

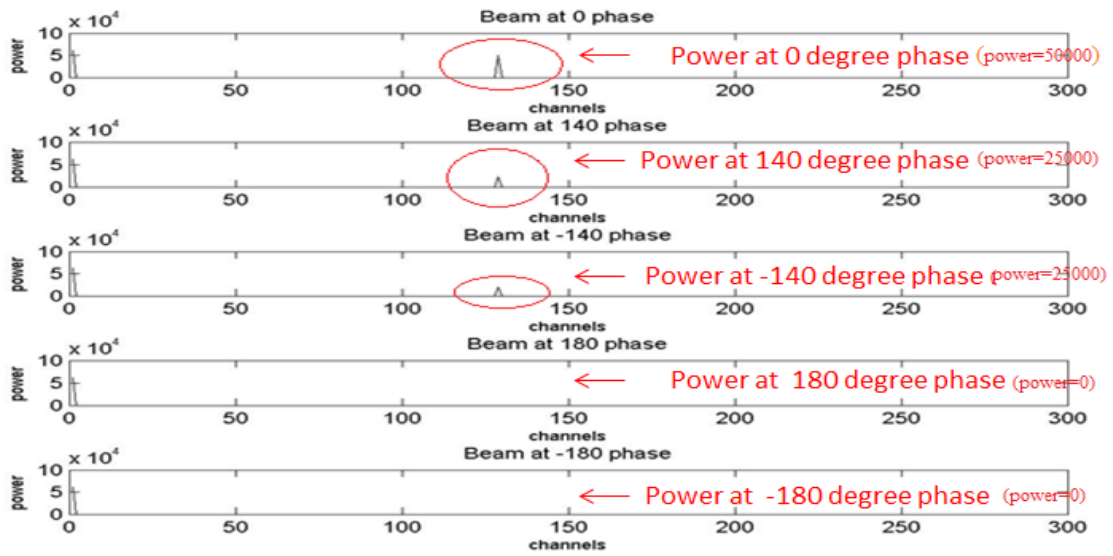


Figure 8.1: Sine wave lab test beamformer output at 0,140,-140,180 and -180 degree phases power vs spectral channels plot

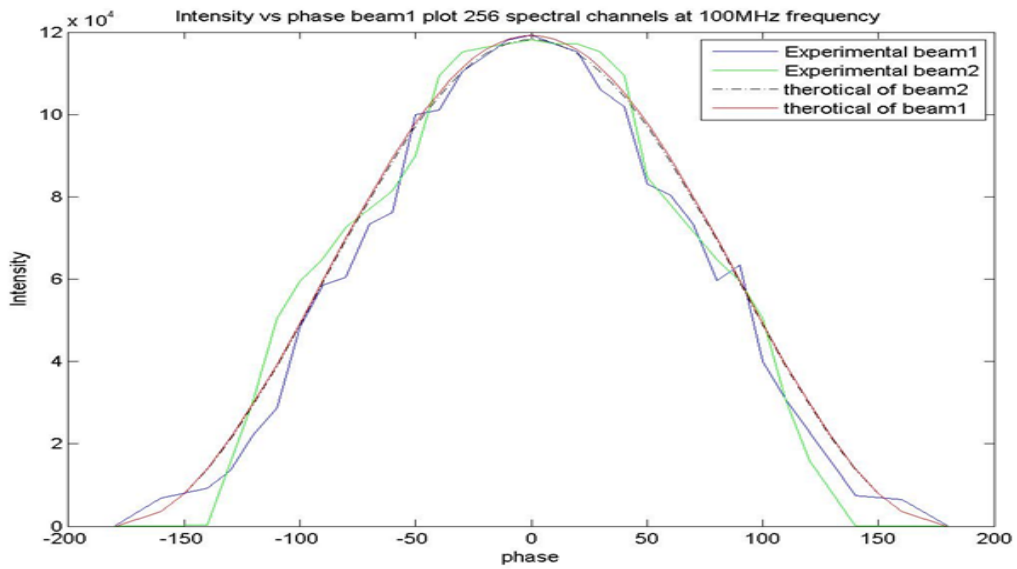


Figure 8.2: Sine wave lab test beamformer output intensity vs phase plot

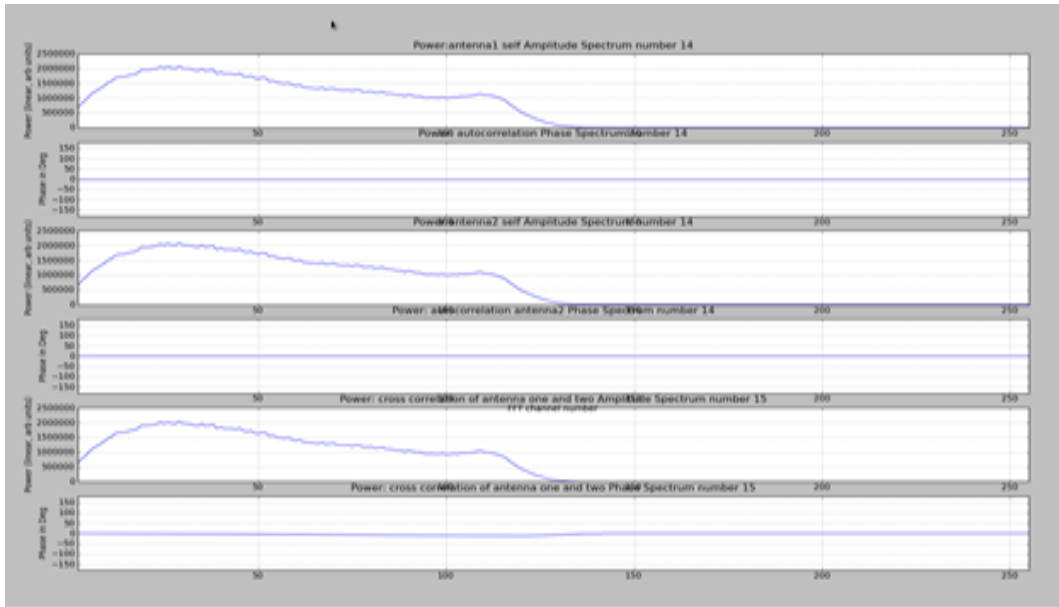


Figure 8.3: Noise source lab test correlator output with both inputs at zero degree phase. First Subplot is self power of first element vs spectral channels, second subplot is self power of second element vs spectral channels, third subplot is first and second elements cross-correlation power vs spectral channels and fourth subplot is cross-correlation phase vs spectral channels.

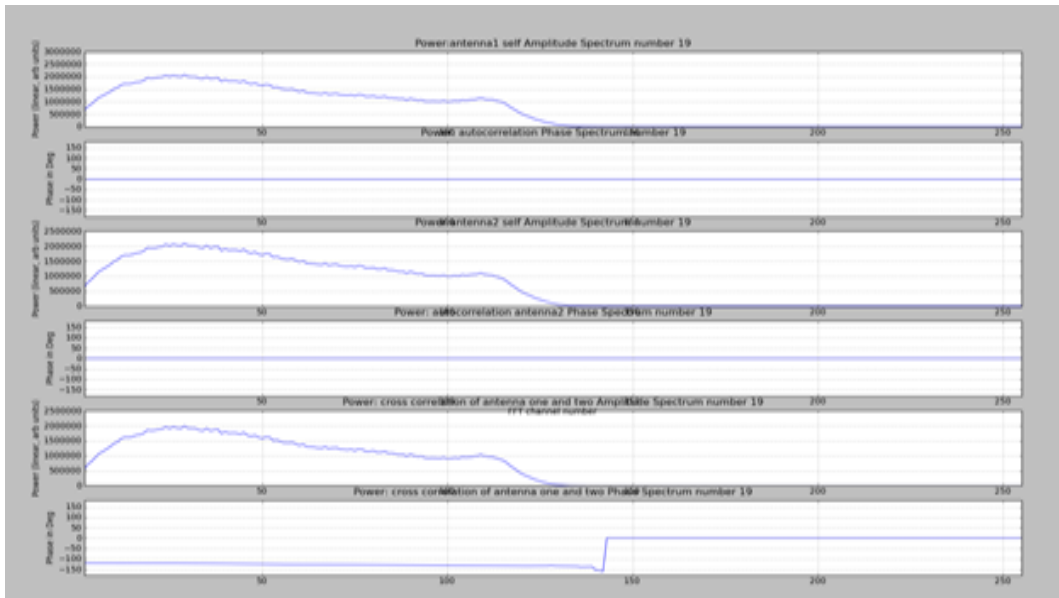


Figure 8.4: Noise source lab test correlator output one input at zero degree phase and another at -120 degree phase. First Subplot is self power of first element vs spectral channels, second subplot is self power of second element vs spectral channels, third subplot is first and second elements cross-correlation power vs spectral channels and fourth subplot is cross-correlation phase vs spectral channels.

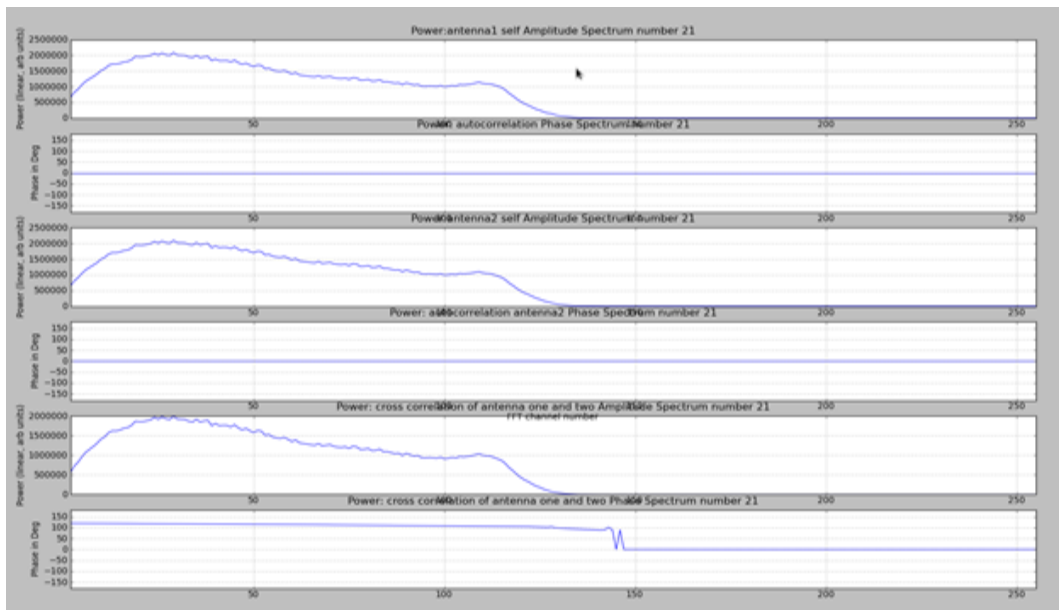


Figure 8.5: Noise source lab test correlator output one input at zero degree phase and another at 120 degree phase. First Subplot is self power of first element vs spectral channels, third subplot is self power of second element vs spectral channels, fifth subplot is first and second elements cross-correlation power vs spectral channels and sixth subplot is cross-correlation phase vs spectral channels.

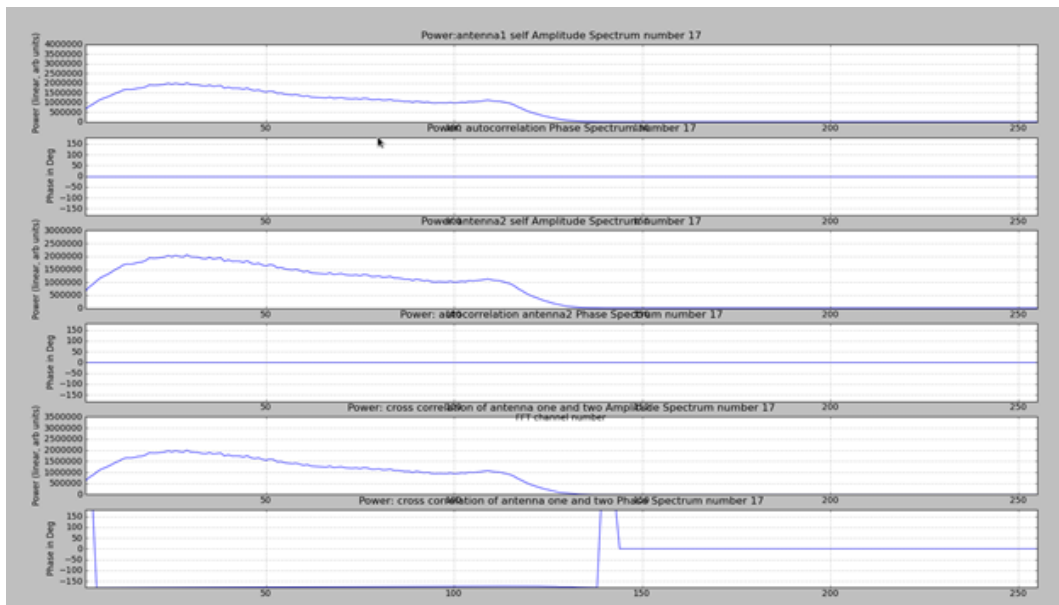


Figure 8.6: Noise source lab test correlator output one input at zero degree phase and another at -180 degree phase. First Subplot is self power of first element vs spectral channels, third subplot is self power of second element vs spectral channels, fifth subplot is first and second elements cross-correlation power vs spectral channels and sixth subplot is cross-correlation phase vs spectral channels.

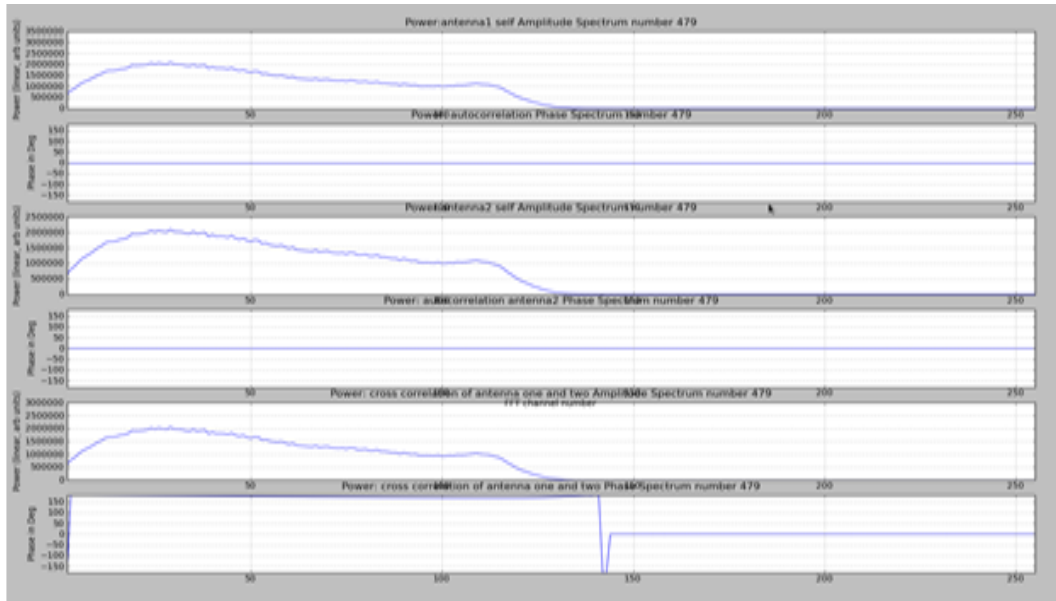


Figure 8.7: Noise source lab test correlator output one input at zero degree phase and another at 180 degree phase. First subplot is self power of first element vs spectral channels, third subplot is self power of second element vs spectral channels, fifth subplot is first and second elements cross-correlation power vs spectral channels and sixth subplot is cross-correlation phase vs spectral channels.

8.1.4 Case4: Check coherent sum block correlated noise as an input with different number of antennas

Description: Apply four correlated noise signals as an input to the design. Before coherent sum using antenna selection logic select number of antennas one to four and record beam data at every step.

Results: Analysis: Coherent sum of four antenna signals is four times the amplitude of the noise signal as shown in figure 8.8. This indicates that the coherent sum block is working.

8.2 GMRT antenna test

8.2.1 Case1: Analyze the effect of phase correction on GMRT antenna signal on correlator output

Description: Apply single input two polarization signals to the design because focal plane array elements are placed very close to each other therefore delay correction part is not included in design. Record cross correlation phase value and apply these phases as a weight to the antenna. Record correlator data after and before phase correction.

Results: Analysis: After phase correction the cross correlation phase becomes zero. Refer figure 8.9 and figure 8.10.

8.3 FPA test

8.3.1 Case1: FPA element selection for radiation test using directional antenna

Description: By radiating a tone signal at 1.1 GHz at -5 dBm power level, check DCU input/output power level.

Mapping and testing table for selected FPA elements: Refer table 8.1

Analysis: Tested all selected elements are working or not as shown in figure 8.11. We get approximately

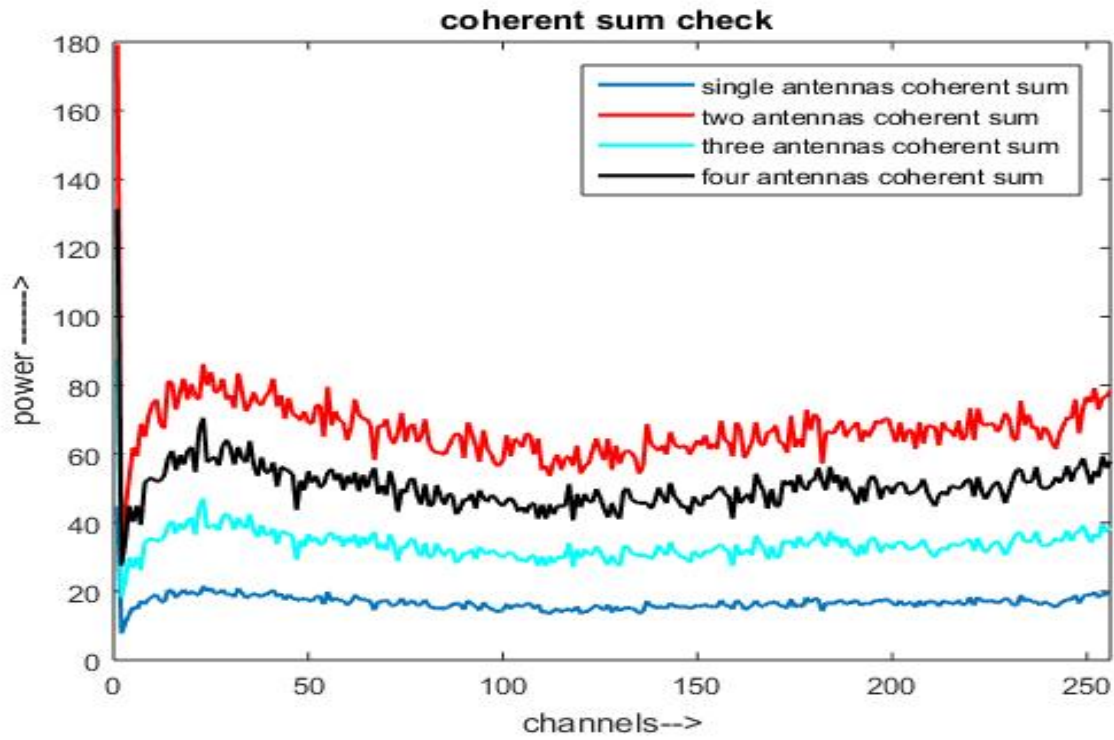


Figure 8.8: Noise source lab test beam output with different number of antennas, power vs spectral channels plot

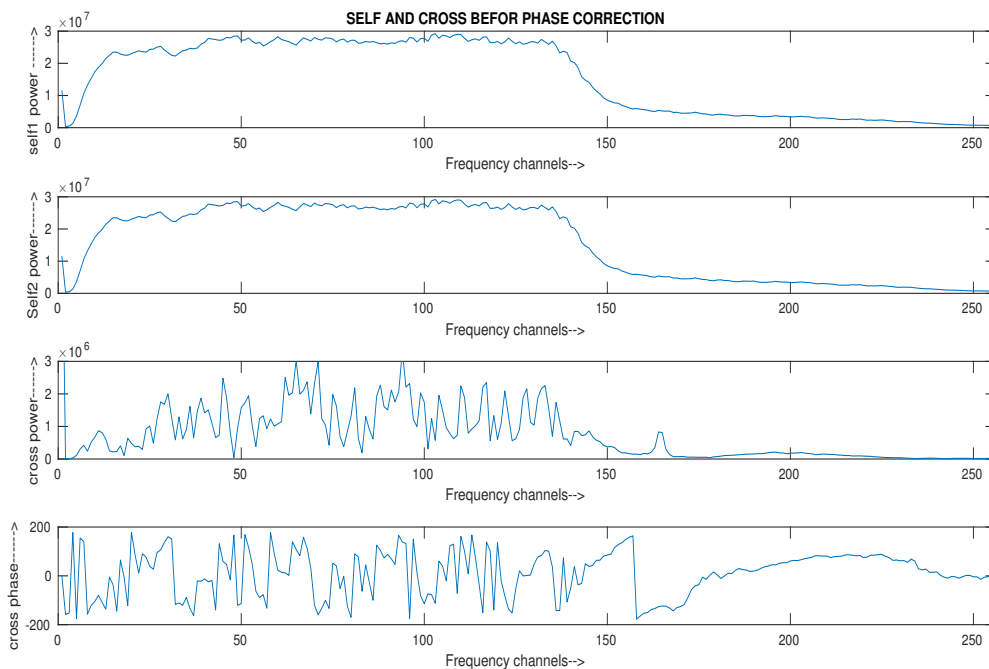


Figure 8.9: Antenna test at 610MHz band source 3C48 correlator output without phase correction
 First Subplot is self power of first element vs spectral channels, second subplot is self power of second element vs spectral channels, third subplot is first and second elements cross-correlation power vs spectral channels and fourth subplot is cross-correlation phase vs spectral channels.

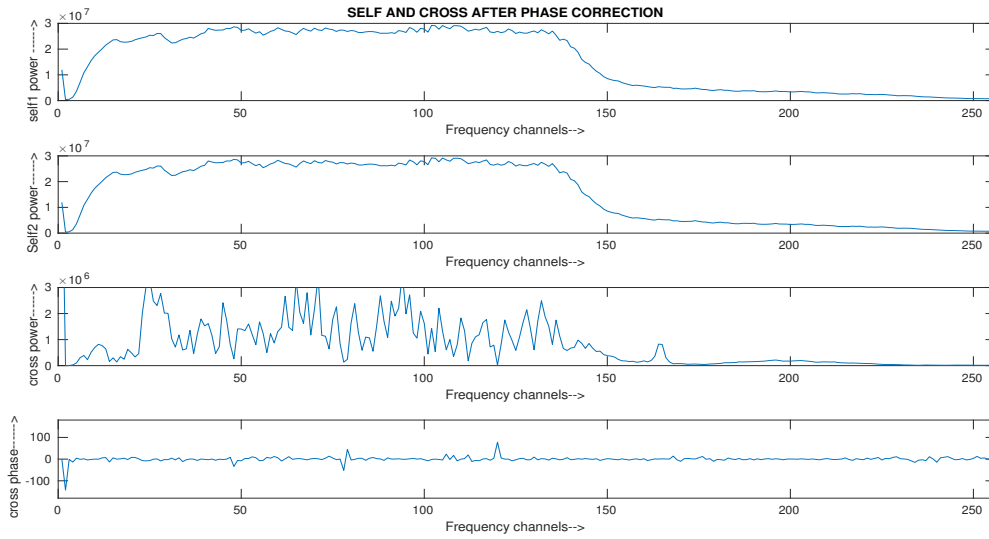


Figure 8.10: Antenna test at 610MHz band source 3C48 correlator output with phase correction
 First Subplot is self power of first element vs spectral channels, second subplot is self power of second element vs spectral channels, third subplot is first and second elements cross-correlation power vs spectral channels and fourth subplot is cross-correlation phase vs spectral channels.

Ax1	Ax2	Ax3	Ax4	Ax5	Ax6	Ax7	Ax8
Bx1	Bx2	Bx3	Bx4	Bx5	Bx6	Bx7	Bx8
Cx1	Cx2	Cx3	Cx4	Cx5	Cx6	Cx7	Cx8
Dx1	Dx2	Dx3	Dx4	Dx5	Dx6	Dx7	Dx8
Ex1	Ex2	Ex3	Ex4	Ex5	Ex6	Ex7	Ex8
Fx1	Fx2	Fx3	Fx4	Fx5	Fx6	Fx7	Fx8
Gx1	Gx2	Gx3	Gx4	Gx5	Gx6	Gx7	Gx8
Hx1	Hx2	Hx3	Hx4	Hx5	Hx6	Hx7	Hx8
Ix1	Ix2	Ix3	Ix4	Ix5	Ix6	Ix7	Ix8

 Tested elements

Figure 8.11: FPA element selection

Table 8.1: DCU power analysis

Feed element no.	DCU input no.	DCU input power (dBm)	DCU output power (dBm)
Dx1	6	-43	-33
Dx2	3	-46	-34
Dx2	45	-46	-34
Dx2	38	-46	-32
Dx2	26	-42	-32
Dx2	24	-43	-32
Dx2	19	-46	-35
Dx2	16	-44	-32
Dx2	58	-43	-32
Dx2	20	-42	-33
Dx2	42	-39	-28
Dx2	28	-46	-33
Dx2	29	-46	-34
Dx2	37	-44	-34

11dB gain at the output of DCU.

8.3.2 Case2: Analyze effect of phase multiplication on correlator output by radiation test

Description: Radiate tone signal at 1.1GHz at -5dBm power level by omnidirectional antenna. Captured this signal using 8x9 Focal Plane Array feed and using down conversion unit(DCU) converted this RF signal in to base band signal at 150MHz. Apply this tone signal to FPGA setup. Record cross correlation phase value and apply these phase as a weight to the antenna. Record correlator data after and before phase correction Refer figure8.12 and figure8.13.

Result: Analysis: After phase correction or weight multiplication cross correlation phase become zero.

8.3.3 Case3: Analyze the effect of phase correction on beam output

Description: Radiate tone signal at 1.1GHz at -5dBm power level by omnidirectional antenna. Captured this signal using 8x9 Focal Plane Array feed and using down conversion unit(DCU) converted this RF signal in to base band signal at 150MHz. Apply this tone signal to the wideband beamformer FPGA setup. Record cross correlation phase value and apply these phase to the corresponding antenna. Record beamformer data after and before phase correction.

Result: Analysis: After phase correction observed improvement in power because after phase correction all signals are in-phase as shown in figure8.14.

8.3.4 Case4: Beam select by applying progressive phase

Description: By selecting four elements of FPA which are horizontal to the ground to avoid ground reflections and radiating tone signal at 1.1GHz (-5dBm). Flow Following steps to steer beam:

- 1) Record phase difference between each element with respect to first element.
- 2) Correct phase and record beam data.
- 3) Record beam output of each element at zero phase without weights.
- 4) Apply progressive 30 degree phase, i.e 30 degree phase to 2nd element, 60 degree phase to 3rd element and 90 degree phase to 4th element and record beam data and beam data as shown in figure8.19.
- 5) Similarly apply 60 degree progressive phase and record beam data.
- 6) Simulate four antenna array with cosine theta as an element pattern and 11cm element spacing using

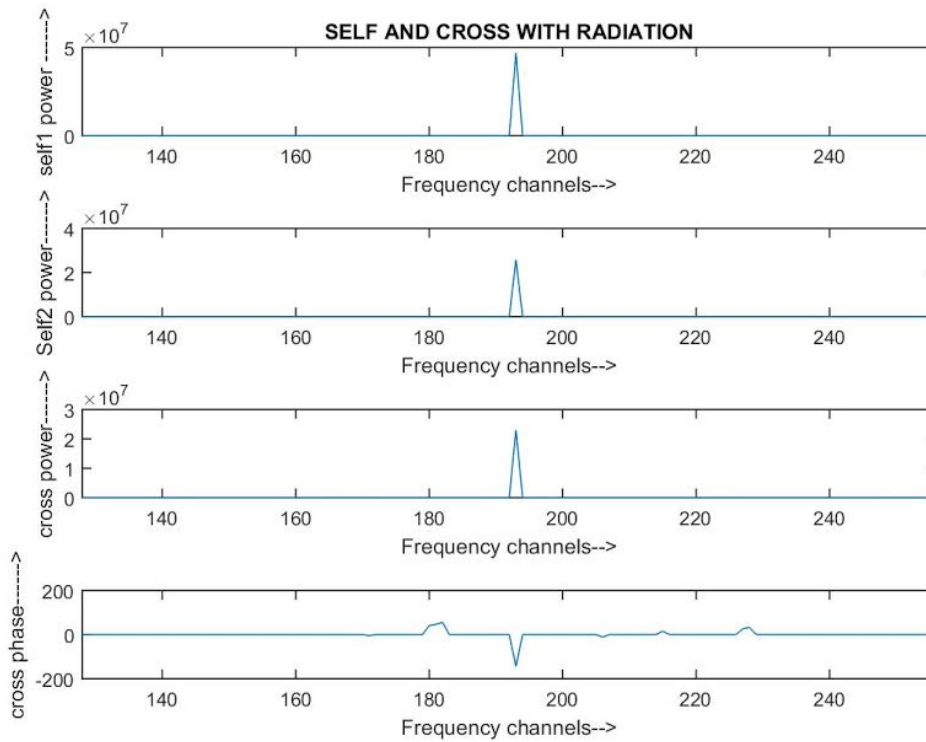


Figure 8.12: FPA setup radiation test correlator output without phase correction
 First Subplot is self power of first element vs spectral channels, second subplot is self power of second element vs spectral channels, third subplot is first and second elements cross-correlation power vs spectral channels and fourth subplot is cross-correlation phase vs spectral channels.

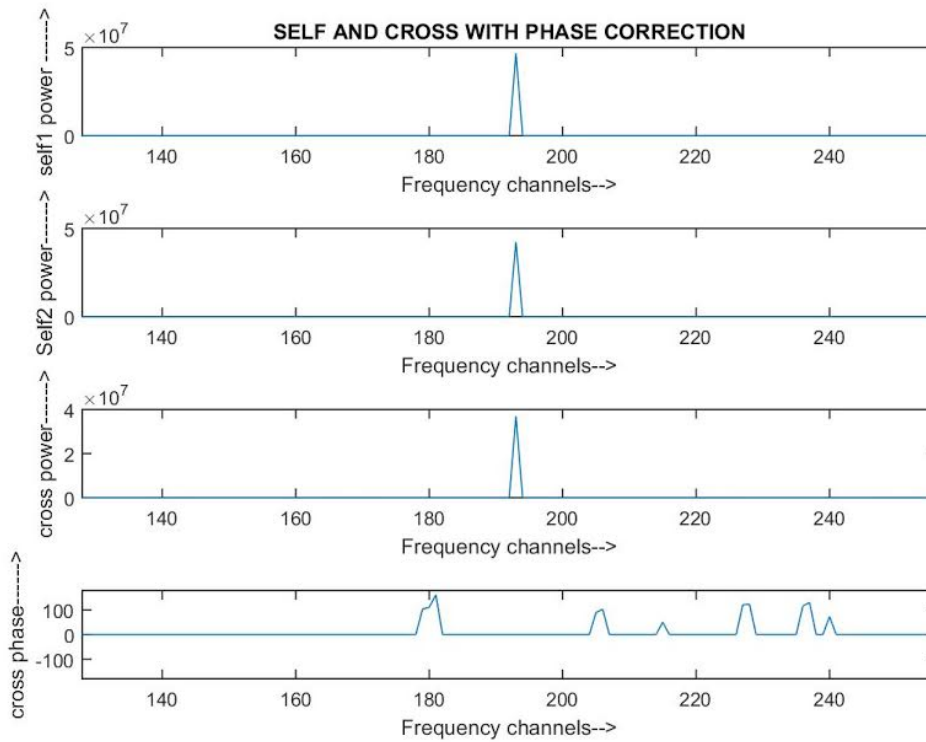


Figure 8.13: FPA test correlator output with phase correction

First Subplot is self power of first element vs spectral channels, second subplot is self power of second element vs spectral channels, third subplot is first and second elements cross-correlation power vs spectral channels and fourth subplot is cross-correlation phase vs spectral channels.

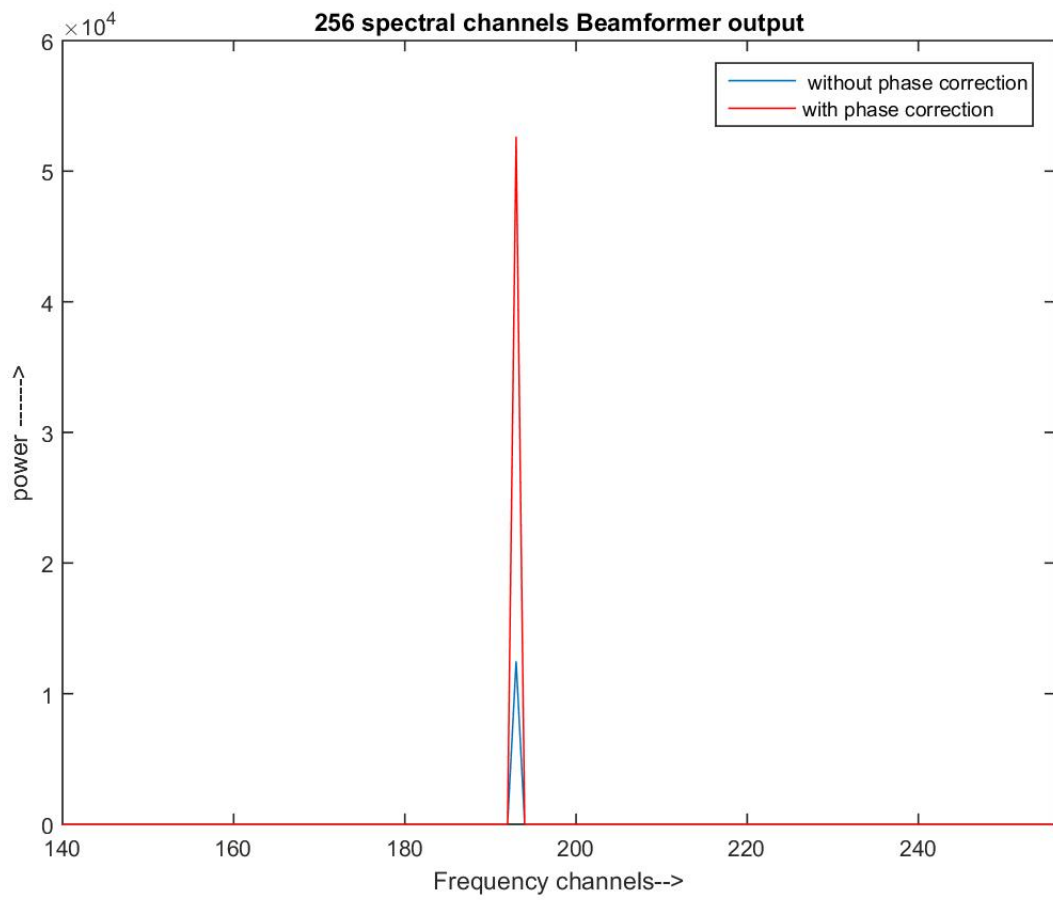


Figure 8.14: FPA setup radiation test beamformer output to observe phase correction effect power vs spectral channels plot

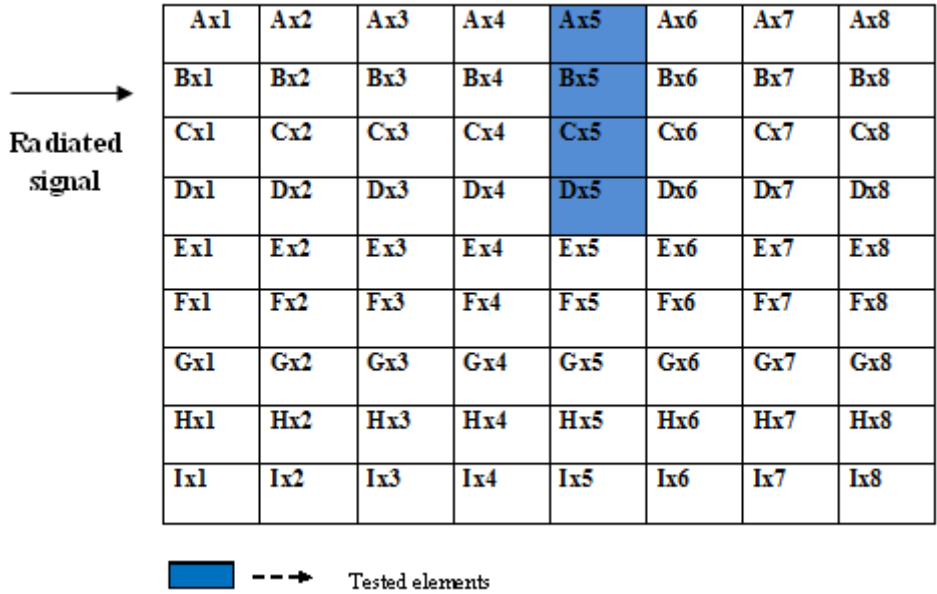


Figure 8.15: FPA element selected for radiation test

pattern multiplication method.

7) Compare simulation output at 30degree, 60degree and 90degree steering angle with obtain results as shown in figure8.16, figure8.17 and figure8.18.

Selected elements for test: refer figure8.15

Analysis: Analyze the effect of steering angle on intensity. Plot beam output at 30 degree, 60degree and 90degree steering angle. At zero degree beam is broad side therefore get maximum amplitude.

8.4 Offline correlation single-board test with internal sync signal

Description: Radiate tone signal at 1.1GHz at -5dBm power level by omnidirectional antenna. Captured this signal using 8x9 Focal Plane Array feed and using down conversion unit (DCU) converted this RF signal into base band signal at 150MHz. Apply this tone signal to FPGA setup. Record beam (refer figure8.20) and correlator data (refer figure8.21) through 10GbE and plot it.

Analysis: Offline correlation algorithm is working.

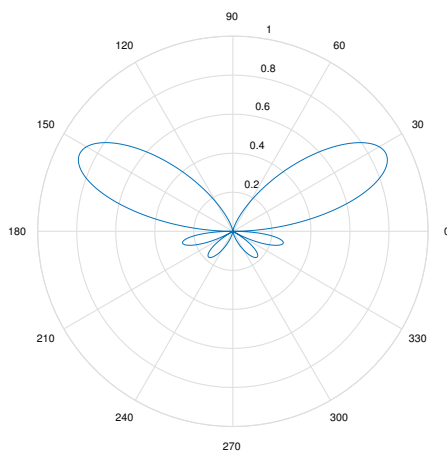


Figure 8.16: Four element simulation using pattern multiplication method at 30 degree steering angle polar plot

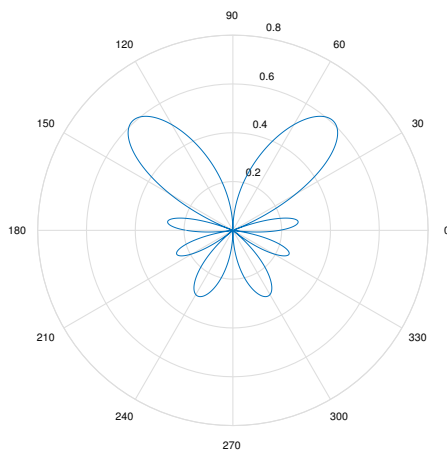


Figure 8.17: Four element simulation using pattern multiplication method at 60 degree steering angle polar plot

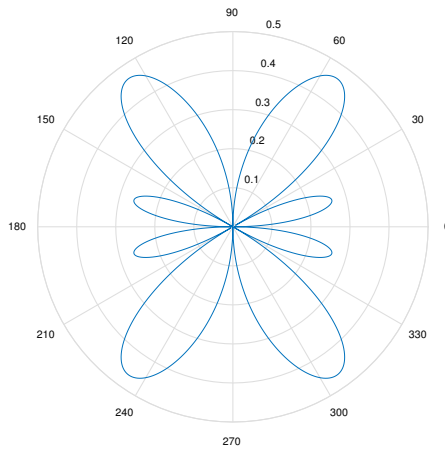


Figure 8.18: Four element simulation using pattern multiplication method at 90 degree steering angle polar plot

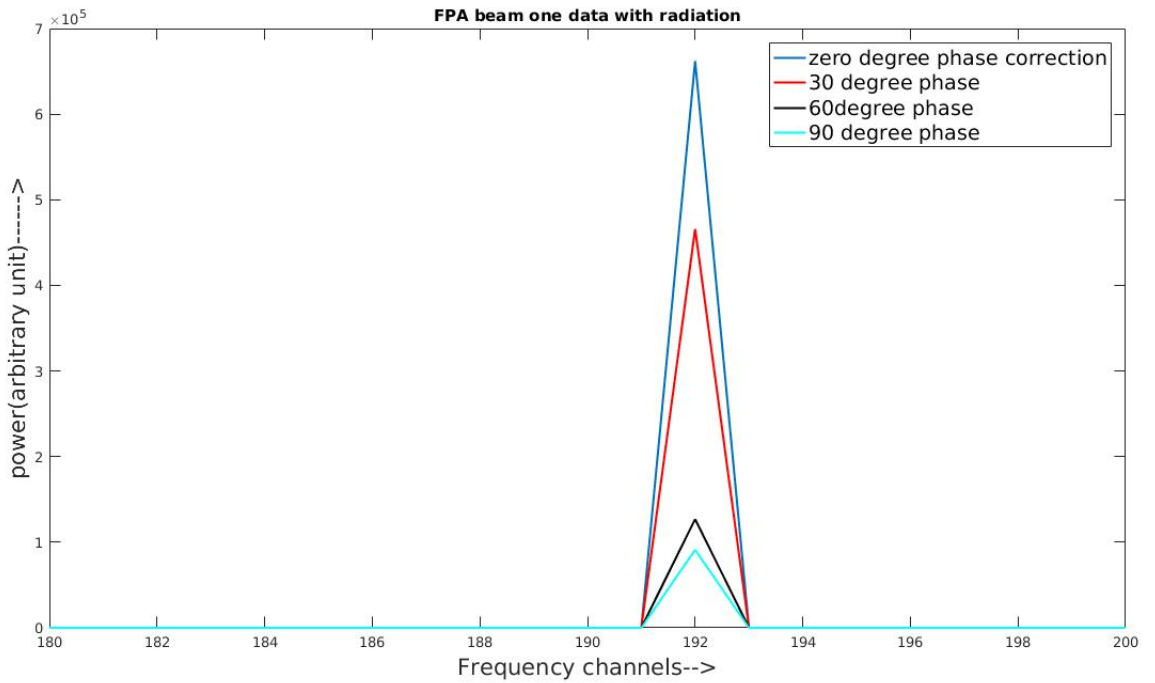


Figure 8.19: Beam output at steering 30degree,60degree and 90degree steering angle power vs spectral channels plot

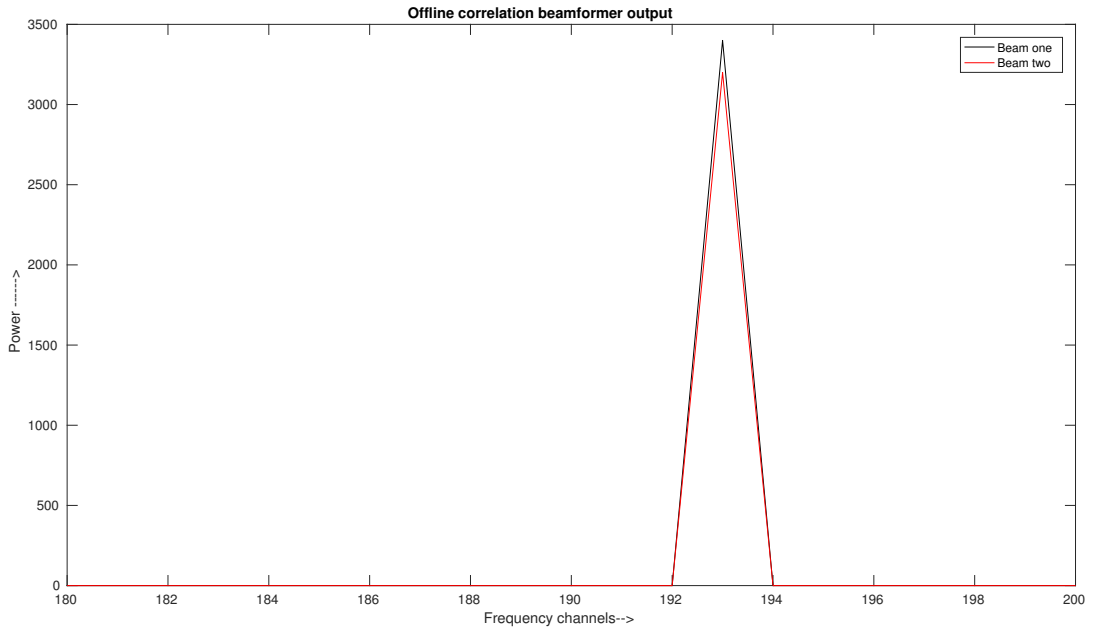


Figure 8.20: Single board(four input)beamformer output power vs spectral channels plot

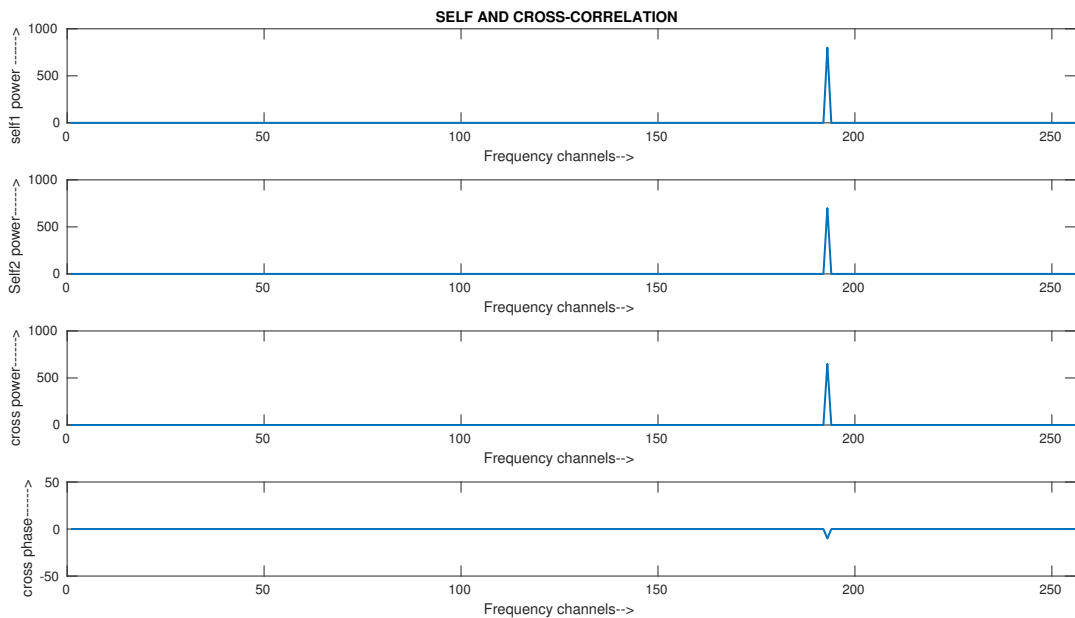


Figure 8.21: Single board(four input)offline correlator output

First Subplot is self power of first element vs spectral channels, second subplot is self power of second element vs spectral channels, third subplot is first and second elements cross-correlation power vs spectral channels and fourth subplot is cross-correlation phase vs spectral channels.

Chapter 9

Conclusion

9.1 Conclusions

Single-board(four-input)beamformer:Four element single polarization two-beam beamformer for focal plane array on single ROACH board has been designed and tested with noise source,GMRT(single pixel feed) antenna and FPA system.

1)The design is tested with weight multiplication algorithm this show the working of phase correction algorithm.

2)With weight multiplication algorithm observed coherent beamformer output (Intensity) by applying different steering angle.

3)Tested coherent sum part with noise source as an input by adding different number of identical inputs observed N times improvement in intensity for inputs. This show signals coherently added.

Scalable architecture:Two board(eight inputs)two-beam beamformer design and tested it for single board(four-input) with internal sync signal by applying sine wave as an input. Checked beamforming algorithm as a part of design.

Four-input four-beam beamformer:In ROACH two enviroment we design this beamformer with high frquency resolution(1024 point FFT).

9.2 Future work

There is a lot of scope for future changes. The following future works are recommended:

1)Design can be tested with focal plane array system with optimal weights

2)The number of FFT points can be improve for higher resolution over the band by implementing design in ROACH2 environment which has more resources than ROACH1.

3)Test scalable architecture two boards correlator and beamformer with external sync signal.

Chapter 10

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