National Centre for Radio Astrophysics
Tata Institute of Fundamental Research
Pune University Campus, Pune -INDIA.

Technical Report on

Design of Clock and Trigger Signal Distribution Unit for GWB System.

Authors:

Navnath Shinde, Ajay Vishwakarma

13 May 2016 _ V1.0

Giant Metrewave Radio Telescope

Khodad- 410504.

Author : Navnath / Ajay **Verified by :**	**Date of issue:**	**Scope**
Approved by: Ajit Kumar B.	**Status/ Version: Ver.1**	**Internal Technical Report No.:**

ACKNOWLEDGEMENT

We are thankful to Prof. Yashwant Gupta (Dean of GMRT) and Prof. S K Ghosh (Center Director of NCRA-TIFR) for giving constant support during this work.

We would also like to express our gratitude towards our group coordinator Shri Ajit Kumar, for his constant guidance and encouragement. We would like to say sincere thanks all our analog and digital lab group member, for time to time sharing and discussing their views for improvement of this developed instrument.

ABSTRACT

The backend receiver system of the Giant Metrewave Radio Telescope (GMRT) is being upgraded and the modifications being implemented in the analog and digital sections of these receivers cater to the improved specifications of the upgraded GMRT (uGMRT).

The main specifications related to the analog section are the ability to process 30 dual polarized RF signals at the central station for a frequency range from 130 to 1600 MHz with seamless frequency coverage, and an instantaneous maximum bandwidth of 400 MHz.

The Digital backend system consists of ROACH board and GPU processors and can easily handle the bandwidth of 400 MHz baseband signal with support up to 16K digital channels.

A very precise and stable Clock & Trigger signal is required for seamless data digitalization purpose. A GPS disciplined Rubidium clock is used to generate reference clock and trigger signal. With an aim of distribution of this reference generated signal, this unit of a system is being developed.

This report describes the design details; implementation scheme and set-up for testing of the Clock and Trigger signal Distribution Unit. It also includes the test results and snapshots of the unit along with datasheets used for the unit.

Sr. No.		Contents	Page No.
1		Introduction	6
2		Design requirement	6
3		Block Diagram	6
4		Circuit Design	7
	4.1	Trigger Signal Distribution	7
	4.2	Clock Signal Distribution	7
5		Specification of IC`s used in Distribution Unit	8
	5.1	IDT 8308A	8
	5.2	8 Way RF Divider(P8-08-454/2S)	8
	5.3	SMPS (NES-25-5)	8
6		Schematic and PCB Layout	9
7		Test and Measurements	10
	7.1	Trigger Signal Distribution	10
	7.2	Clock Signal Distribution	12
8		Bill of Materials	15
9		Snapshots	16
10		Datasheets	17
	10.1	IDT 8308A	17
	10.2	8 Way RF Divider(P8-08-454/2S)	21
	10.3	SMPS (NES-25-5)	22

Fig. No.	Name of Figure	Page No.
Figure 1:	Block Diagram of Clock and Trigger Signal Distribution Unit.	6
Figure 2:	Schematic Diagram of Clock and Trigger Signal Distribution unit.	7
Figure 3:	PCB of Trigger Signal Distribution Unit.	9
Figure 4:	PCB layout Diagram of Trigger Signal Distribution Unit.	9
Figure 5:	Plots of Trigger Signal output (1PPS 50% duty cycle) Distribution Unit.	10
Figure 6:	Rise time of Trigger (1PPS) Input and Output Signal.	10
Figure 7:	Fall time of Trigger (1PPS) Input and Output Signal.	11
Figure 8:	Delay between Input and Output of Trigger (1PPS) Signal.	11
Figure 9:	Plot of 800MHz Clock Signal Distribution Unit.	12
Figure 10:	Plot showing Harmonics of Clock (800MHz) Input Signal.	13
Figure 11:	Plot showing Harmonics of Clock (800MHz) Output Signal.	13
Figure 12:	Snapshots of 8 Way RF Divider Pulsar microwave (P8-08-454/2S).	14
Figure 13:	Transmission loss of 8 Way RF Divider (Pulsar Microwave_P8-08-454/2S).	14
Figure 14:	Reflection loss of 8 Way RF Divider (Pulsar Microwave_P8-08-454/2S).	14
Figure 15:	Bill of Materials for Clock and Trigger Signal Distribution Unit.	15
Figure 16:	Snapshots of Clock and Trigger Signal Distribution Unit.	16

1. Introduction:

The clock and trigger signal are required to the hardware (ROACH Boards) of the upgrade wideband digital back-end (GWB) system to maintain the synchronization in the signal digitalization process. The prerequisite of this signal is that both are generated using the T&F standard of the GMRT. The design helps to make the multiple copies of the reference signal as an input to the GWB digitalizing units.

2. Design Requirement:

1. To provide 8 copies of the Trigger signal either PPS or PPM.
2. To provide 8 copies of the Clock signal having range from 10 MHz to 1500MHz.

3. Block Diagram:

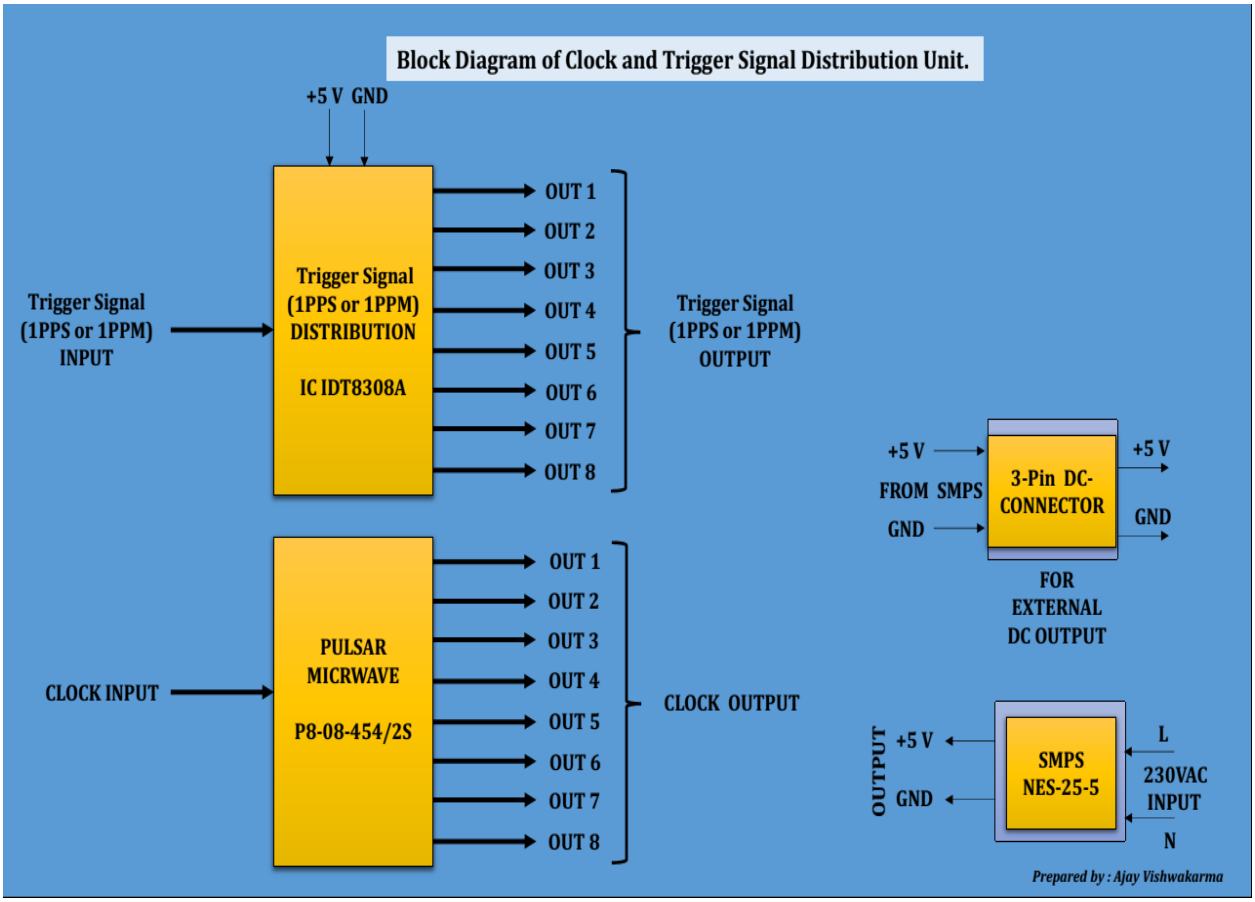


Figure 1: Block Diagram of Clock and Trigger Signal Distribution Unit.

4. Circuit Design:

4.1 Trigger Signal Distribution:

A Trigger signal (PPM/PPS) is received from the Time and frequency standard of the GMRT and this signals are received in the Correlator room. For 1PPS distribution, IDT8308 LVCMOS fan-out buffer IC is used which provide 5V TTL output. This unit operates at + 5V DC from SMPS output. The IDT make ICS8308I has been selected and a circuit designed as shown in the circuit diagram.

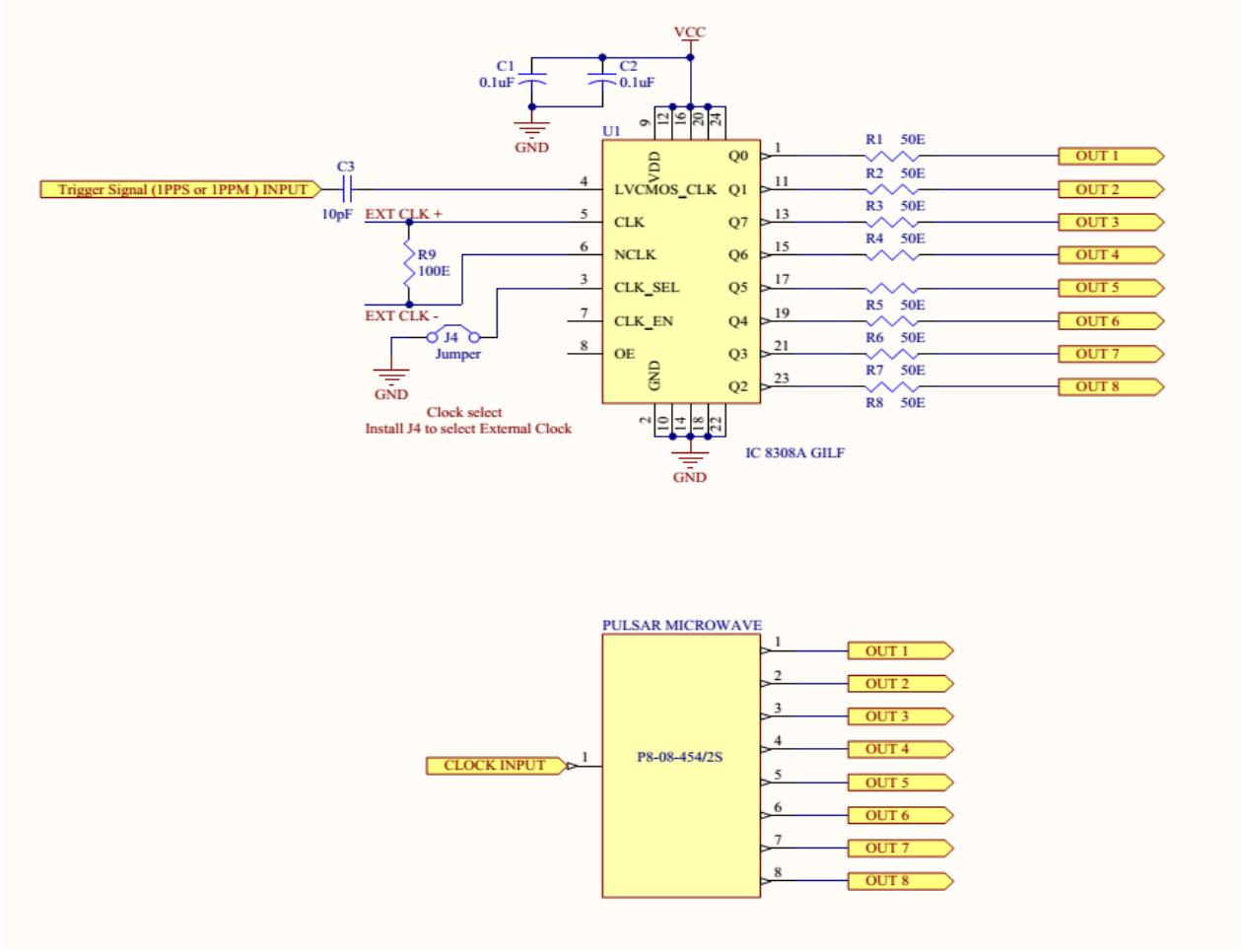


Figure 2: Schematic Diagram of Clock and Trigger Signal Distribution Unit.

4.2 Clock Signal Distribution:

For Clock distribution 8-way Pulsar make divider P8-08-454/2S is used which provides 800MHz Clock output with -14 dBm power level.

A dedicated Meanwell make SMPS is used in this unit. This PIU is integrated in 1U size enclosure which serves as a distribution circuit for both Clock and 1PPS sync Output. The unit operates at 230VAC Input with down converting the power supply to +5V DC through SMPS Unit. This unit is also having features with ON/OFF switch to Mains 230VAC power supply along with Fuse of 2A rating.

5. The specifications of the IC's used in the Distribution unit are as follows:

5.1 IDT 8308A:

1. Low skew,1-to -8 Fan-out buffer
2. Two selectable inputs, (1. CLK and 2. Differential input levels)
3. Outputs are designed to drive 50 ohm series or parallel terminated transmission lines.
4. Eight LVCMOS/LVTTL outputs, (7Ωtypical output impedance
5. Selectable LVCMOS_CLK or differential CLK, nCLK inputs
6. CLK, nCLK pair can accept the following differential input levels: LVPECL, LVDS, LVHSTL, SSTL, HCSL.
7. Guaranteed output and part-part skew characteristics make the 8308I ideal for those clock distribution applications.

5.2 8 Way RF Divider(P8-08-454/2S):

1. Pulsar Microwave Make.
2. Frequency Range: 5 – 2000MHz.
3. Insertion Loss: 4.5 dB Max.
4. Isolation: 16 dB Min.
5. Power: 1 Watt Max.

5.3 SMPS (NES-25-5):

1. Meanwell Make.
2. DC Voltage:5V
3. Rated Current:5A
4. Rated Power:25W
5. Protections: Short circuits/Overload/Over voltage.
6. Single Output switching Power Supply.

6. Schematic and PCB layout:

Altium Designer software is used for making a schematic and PCB layout diagram of Trigger (1PPS/PPM) Signal Distribution circuit. It has one input and 8 multiples output used for Trigger (1PPS or 1PPM) signal distribution. The outputs are matched with 50 ohm series impedance for transmission lines. It requires +5V DC supply for its operations. The size of this PCB is 130x50mm having track width of 1mm with thickness 1.5mm.

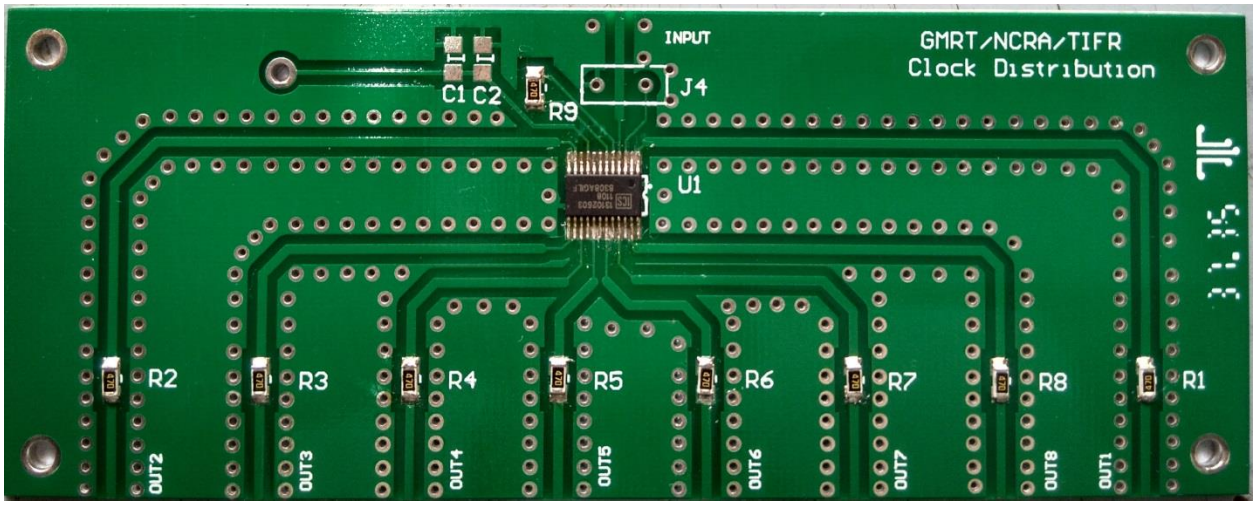


Figure 3: PCB of Trigger Signal Distribution Unit.

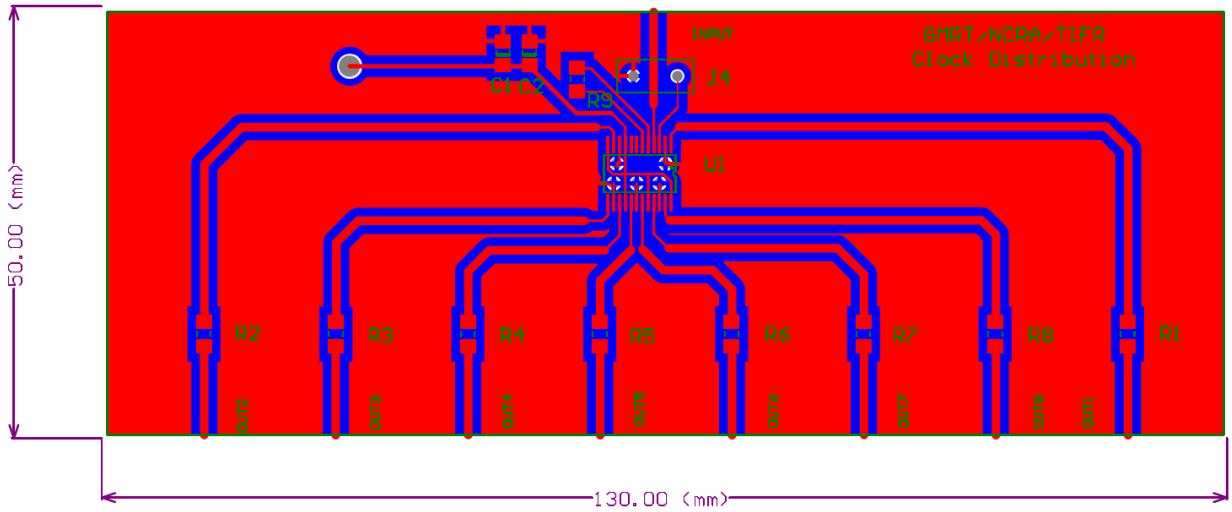


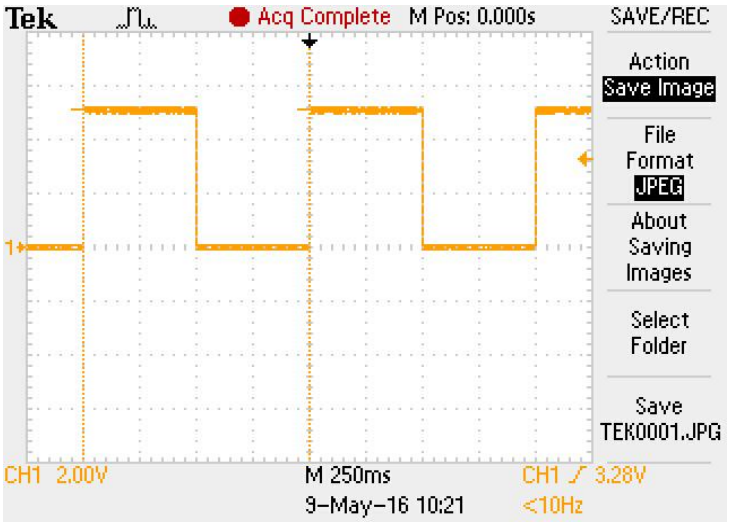
Figure 4: PCB layout Diagram of Trigger Signal Distribution Unit.

7. Test and Measurements:

7.1 Trigger Signal Distribution:

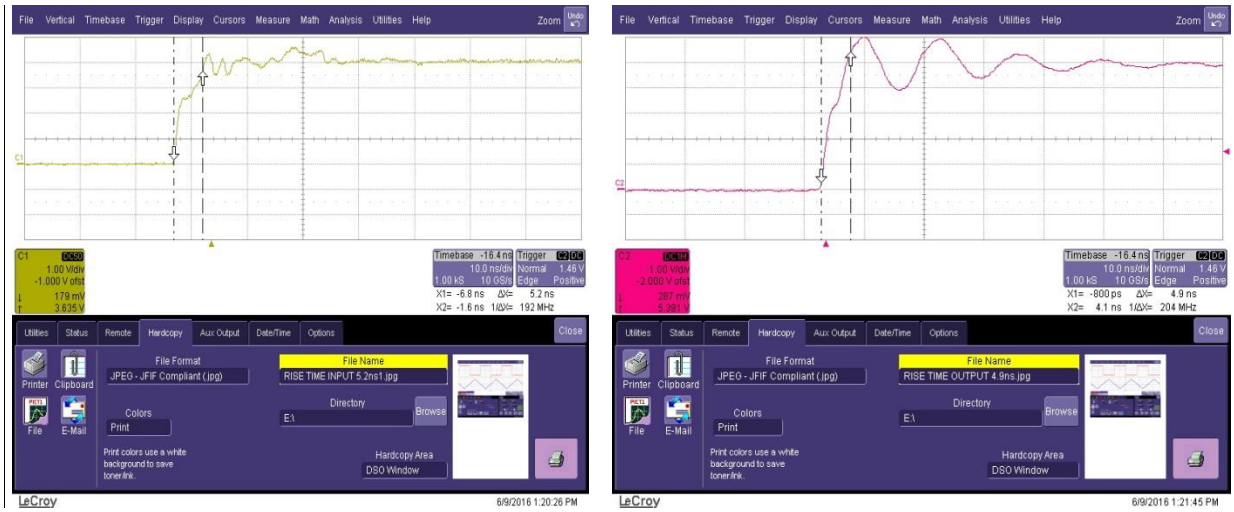
For testing a trigger Signal distribution, A TM4-M/D unit is used which provides a 1PPS (50% duty cycle) output on Port E. This 1PPS input is connected to trigger distribution circuit and 8 multiple copies of 1PPS signal are taken as output.

- **Following are the plots of Trigger Signal (1PPS output) shown below:**



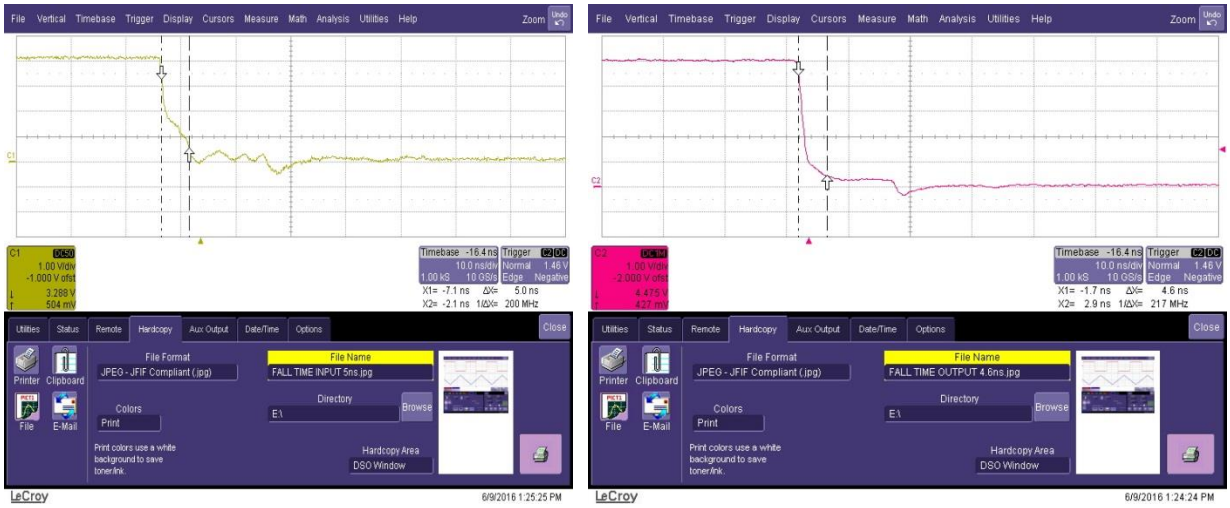
(i) 1PPS Amplitude (5V) and Frequency (1Hz).

Figure 5: Plots of Trigger Signal output (1PPS 50% duty cycle) Distribution Unit.



(i) Rise Time_5.2 ns 1PPS Input Signal. **(ii) Rise Time_4.9 ns 1PPS Output Signal.**

Figure 6: Rise time of Trigger (1PPS) Input and Output Signal.



(i) Fall Time_5.0 ns 1PPS Input Signal **(ii) Fall Time_4.6 ns 1PPS Output Signal**

Figure 7: Fall time of Trigger (1PPS) Input and Output Signal.

(ii) Rise Time Delay_5.8 ns Input Signal **(ii) Fall Time Delay_5.2 ns Output Signal**

Figure 8: Delay between Input and Output of Trigger (1PPS) Signal.
…….CH1_Yellow colour indicates 1PPS Input Signal
…….CH2_Pink colour indicates 1PPS Output Signal.

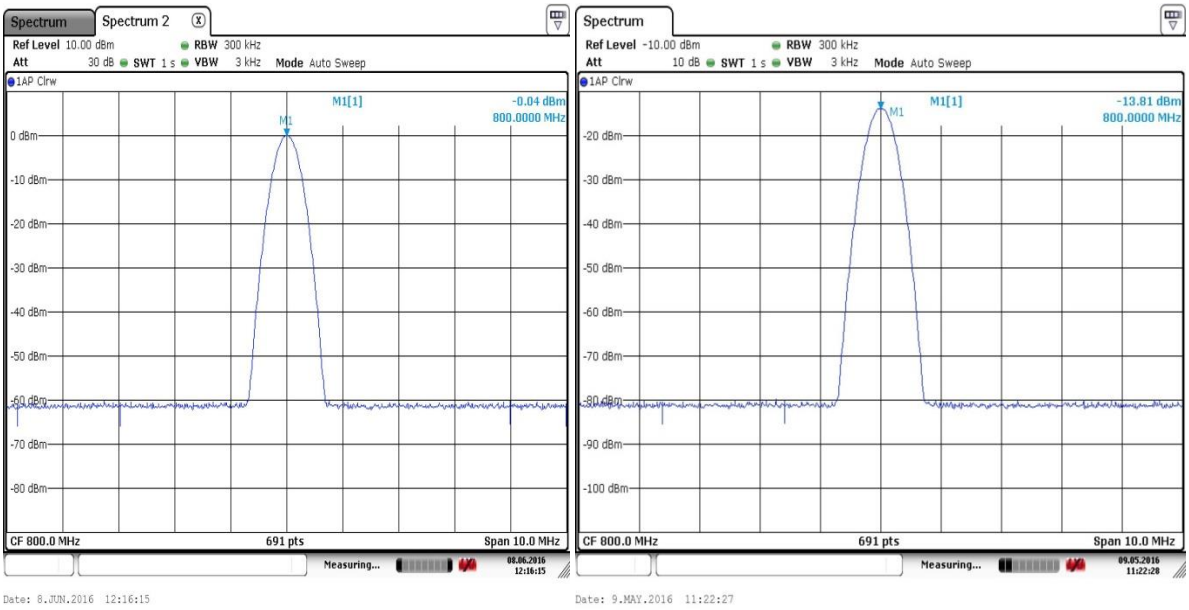
➢ Summary Table:

Sr. No.	Description	1PPS Input Signal	1PPS Output Signal
1	Rise Time	5.2 ns	4.9 ns
2	Fall Time	5.0 ns	4.6 ns
3	Rise Time Delay	5.8 ns	
4	Fall Time Delay	5.2 ns	

7.2 Clock Signal Distribution:

For testing a Clock Signal distribution, a signal Generator SMA100 is used for providing CW Signal of 800MHz Clock as Input to 8-Way RF Divider (Pulsar Microwave_P8-08-454/2S) which gives 8 multiple copies of Clock Signal with -14 dBm power level.

Loss calculated in 8 Way RF Divider (dB) =10*log 8 …… (8=for 8 Way RF Divider)
=10*0.9030
=9dB + (4.5dB) Insertion loss
=13.5dB



(i) 800 MHz Clock Input Signal. **(ii) 800 MHz Clock Output Signal.**

Figure 9: Plot of 800MHz Clock Signal Distribution Unit.

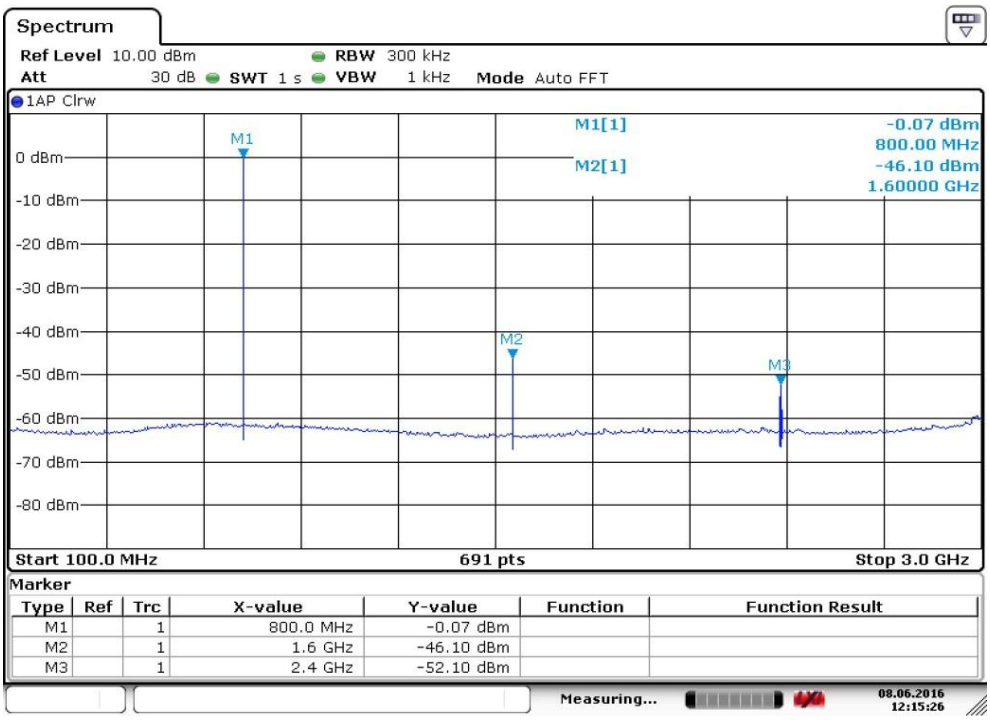


Figure 10: Plot showing Harmonics of Clock (800MHz) Input Signal.

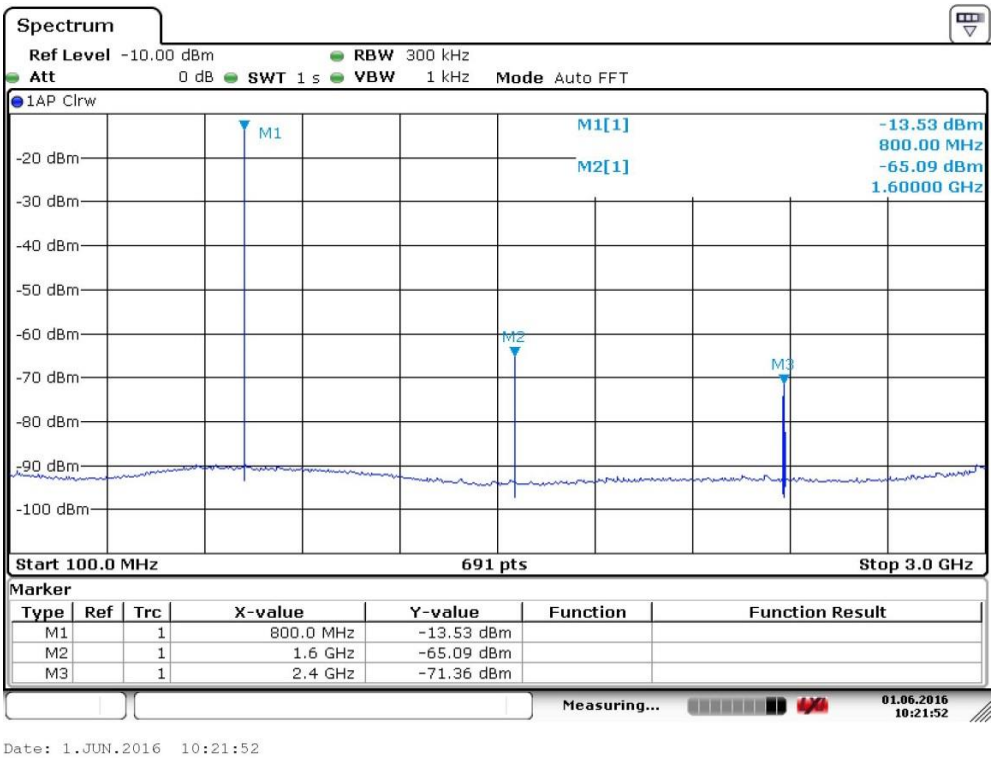


Figure 11: Plot showing Harmonics of Clock (800MHz) Output Signal.

- **8 Way RF Divider(P8-08-454/2S):**

Figure 12: Snapshots of 8 Way RF Divider Pulsar microwave (P8-08-454/2S).

- **Following are the Transmission and Reflection loss of 8 Way RF Divider (Pulsar Microwave P8-08-454/2S).**

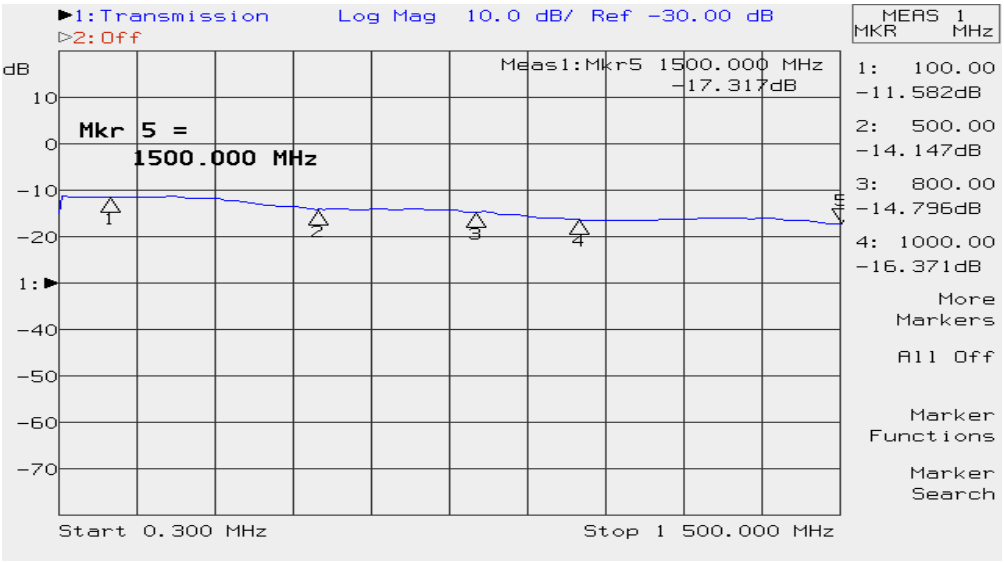


Figure 13: Transmission loss of 8 Way RF Divider (Pulsar Microwave_P8-08-454/2S).

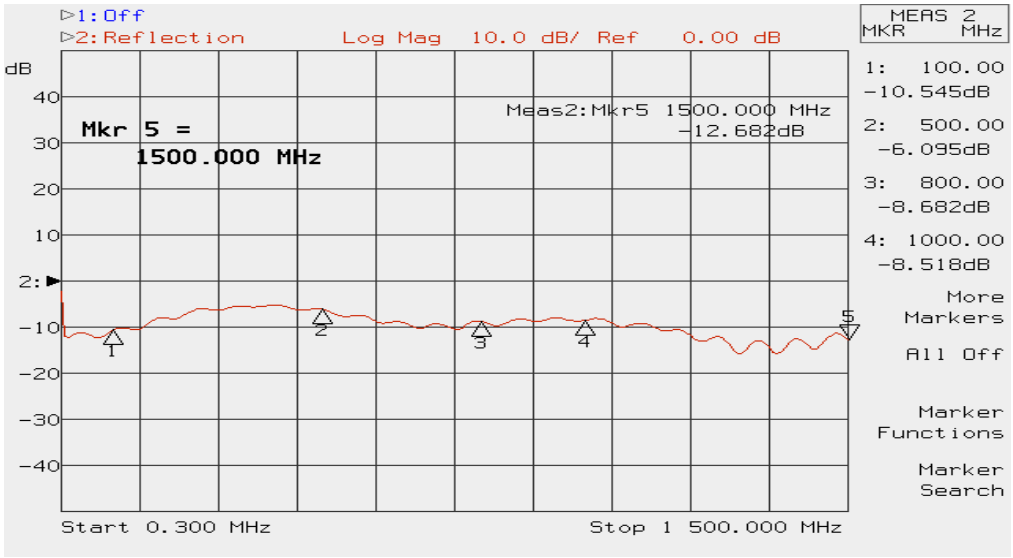


Figure 14: Reflection loss of 8 Way RF Divider (Pulsar Microwave_P8-08-454/2S).

8. Bill of Materials:

	Bill of Materials for Clock Signal Distribution PCB				
SR No.	**Description**	**Type / Make**	**Designator**	**Value**	**Quantity**
1	Capacitor	SMD	C1, C2	0.1uF	2
		SMD	C3	10pF	1
2	Resistor	SMD	R1,R2,R3,R4,R5,R6,R7,R8	50E, 1/4W	8
		SMD	R9	100E, 1/4W	1
3	Jumper	Plastic	J4	Link	1

	Bill of Materials for Clock & Trigger Signal Distribution Unit			
SR No.	**Description**	**Make**	**Type**	**Quantity**
1	SMA Connector	Huber-Suhner	Straight Panel Cable Jack-Female	10
2	SMA Connector	Huber-Suhner	Straight Panel Cable Jack-Male	2
3	SMA Connector	Huber-Suhner	Straight Bulkhead Cable Jack-Female	1
4	DC Connector		DC power Connector - 3Pin	1
5	Clock PCB	FR4 Board	Designed PCB	1
6	8 Way RF Divider	Pulsar Microwave	Inductive module	1
7	1U Unit (19" Size)	Home made	Aluminium Box	1
8	230V AC Switch		Plastic	1

Figure 15: Bill of Materials for Clock and Trigger Signal Distribution Unit.

9. Snapshots:

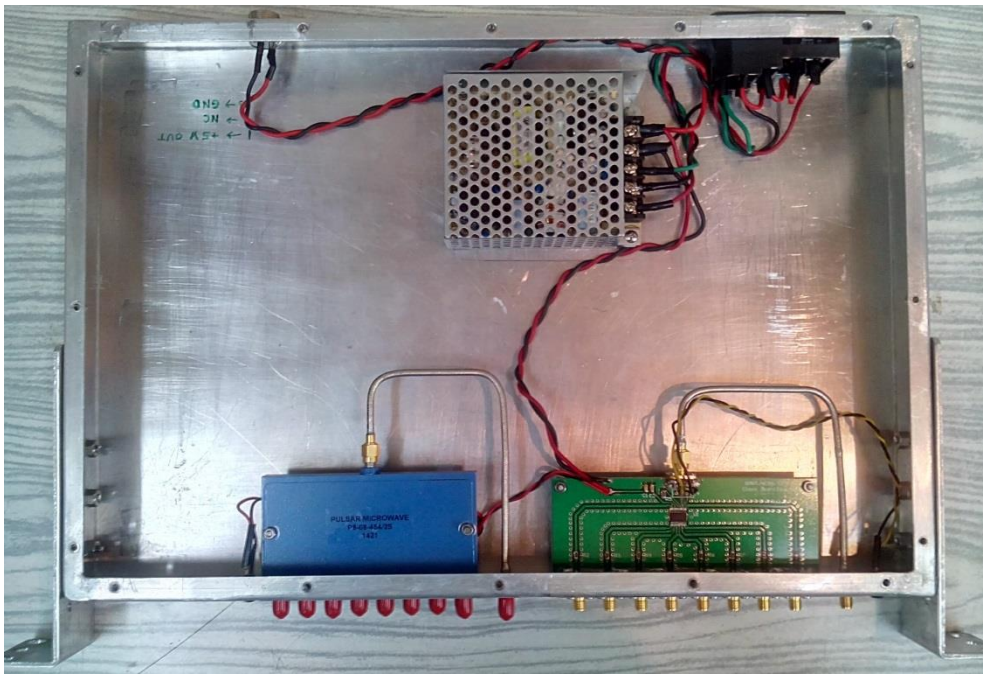
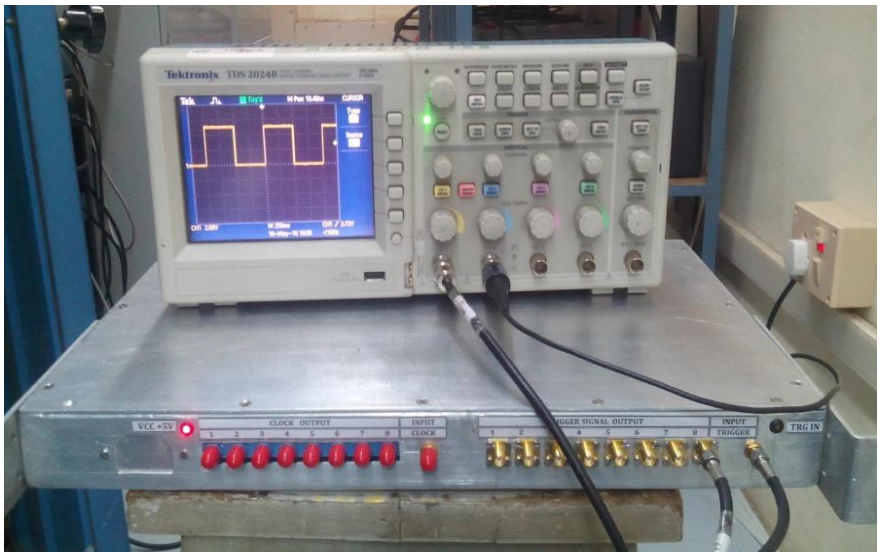


Figure 16: Snapshots of Clock and Trigger Signal Distribution Unit.

Front view

Rear view



Set-up for testing Trigger Signal Distribution Unit

10. Datasheets:

10.1 IDT 8308A:

IDT

Low Skew, 1-to-8 Differential/LVCMOS-to-LVCMOS Fanout Buffer

ICS8308I

DATA SHEET

General Description

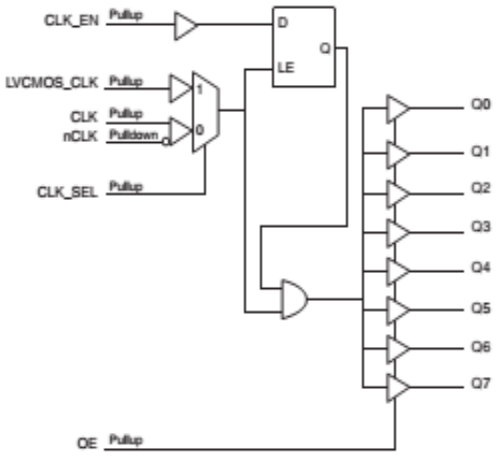
The ICS8308I is a low-skew, 1-to-8 Fanout Buffer. The ICS8308I has two selectable clock inputs. The CLK, nCLK pair can accept most differential input levels. The LVCMOS_CLK can accept LVCMOS or LVTTL input levels. The low impedance LVCMOS/LVTTL outputs are designed to drive 50Ω series or parallel terminated transmission lines. The effective fanout can be increased from 8 to 16 by utilizing the ability of the outputs to drive two series terminated transmission lines.

The ICS8308I is characterized for 3.3V core/3.3V output, 3.3V core/2.5V output or 2.5V core/2.5V output operation. Guaranteed output and part-part skew characteristics make the 8308I ideal for those clock distribution applications requiring well defined performance and repeatability.

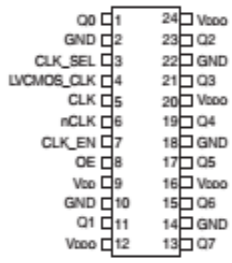
Features

- Eight LVCMOS/LVTTL outputs, (7Ω typical output impedance)
- Selectable LVCMOS_CLK or differential CLK, nCLK inputs
- CLK, nCLK pair can accept the following differential input levels: LVPECL, LVDS, LVHSTL, SSTL, HCSL
- Maximum Output Frequency: 350MHz
- Output Skew: (3.3V± 5%): 100ps (maximum)
- Part to Part Skew: (3.3V± 5%): 1ns (maximum)
- Supply Voltage Modes:
  (Core/Output)
  3.3V/3.3V
  3.3V/2.5V
  2.5V/2.5V
- -40°C to 85°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

Block Diagram



Pin Assignment



ICS8308I
24-Lead, 173-MIL TSSOP
4.4mm x 7.8mm x 0.925mm body package
G Package
Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 11, 13, 15, 17, 19, 21, 23	Q0, Q1, Q7, Q6, Q5, Q4,Q3, Q2	Output		Clock outputs. LVCMOS / LVTTL interface levels.
2, 10, 14, 18, 22	GND	Power		Power supply ground.
3	CLK_SEL	Input	Pullup	Clock select input. Selects LVCMOS clock input when HIGH. Selects CLK, nCLK inputs when LOW. See Table 3A. LVCMOS / LVTTL interface levels.
4	LVCMOS_CLK	Input	Pullup	Clock input. LVCMOS / LVTTL interface levels.
5	CLK	Input	Pullup	Non-inverting differential clock input.
6	nCLK	Input	Pulldown	Inverting differential clock input.
7	CLK_EN	Input	Pullup	Clock enable. LVCMOS / LVTTL interface levels.
8	OE	Input	Pullup	Output enable. LVCMOS / LVTTL interface levels. See Table 3B.
9	V_{DD}	Power		Power supply pin.
12, 16, 20, 24	V_{DDO}	Power		Output supply pins.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
C_{PD}	Power Dissipation Capacitance (per output)			12		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
R_{OUT}	Output Impedance		5	7	12	Ω

TABLE 3A. CLOCK SELECT FUNCTION TABLE

Control Input	Clock Input
CLK_SEL	
0	CLK, nCLK is selected
1	LVCMOS_CLK is selected

TABLE 3B. OE SELECT FUNCTION TABLE

Control Input	Output Operation
OE	
0	Outputs Q0:Q7 are in Hi-Z (disabled)
1	Outputs Q0:Q7 are active (enabled)

TABLE 3C. CLOCK INPUT FUNCTION TABLE

Inputs				Outputs	Input to Output Mode	Polarity
CLK_SEL	LVCMOS_CLK	CLK	nCLK	Q0:Q7		
0	—	0	1	LOW	Differential to Single Ended	Non Inverting
0	—	1	0	HIGH	Differential to Single Ended	Non Inverting
0	—	0	Biased; NOTE 1	LOW	Single Ended to Single Ended	Non Inverting
0	—	1	Biased; NOTE 1	HIGH	Single Ended to Single Ended	Non Inverting
0	—	Biased; NOTE 1	0	HIGH	Single Ended to Single Ended	Inverting
0	—	Biased; NOTE 1	1	LOW	Single Ended to Single Ended	Inverting
1	0	—	—	LOW	Single Ended to Single Ended	Non Inverting
1	1	—	—	HIGH	Single Ended to Single Ended	Non Inverting

NOTE 1: Please refer to the Application Information section, "Wiring the Differential Input to Accept Single Ended Levels".

Schematic Example

Figure 3 shows a schematic example of the ICS8308I. In this example, the LVCMOS_CLK input is selected. The decoupling capacitors should be physically located near the power pin.

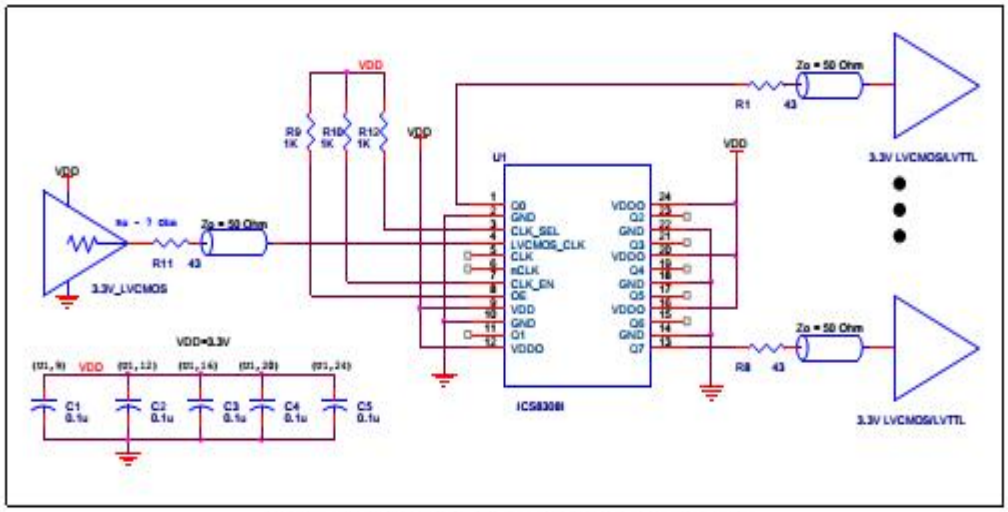


FIGURE 3. ICS8308I LVPECL BUFFER SCHEMATIC EXAMPLE

Recommendations for Unused Input and Output Pins

Inputs:

LVCMOS_CLK Input

For applications not requiring the use of an LVCMOS_CLK, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the LVCMOS_CLK input to ground.

CLK/nCLK Inputs

For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground.

LVCMOS Control Pins

All control pins have internal pullups or pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVCMOS Outputs

All unused LVCMOS outputs can be left floating. There should be no trace attached.

Power On Sequence

There is no power on sequence requirement for the V_{DD} and V_{DDO}. If the V_{DDO} is turned on before the V_{DD} there will be unknown state at the outputs during initial condition when the V_{DDO} is on and V_{DD} is off.

Reliability Information

Table 6. θ_{JA} vs. Air Flow Table for 24 Lead TSSOP

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	200	500
Multi-Layer PCB, JEDEC Standard Test Boards	70°C/W	63°C/W	60°C/W

Transistor Count

The transistor count for ICS8308I is: 1040

Package Outline and Dimensions

Package Outline - G Suffix for 24 Lead TSSOP

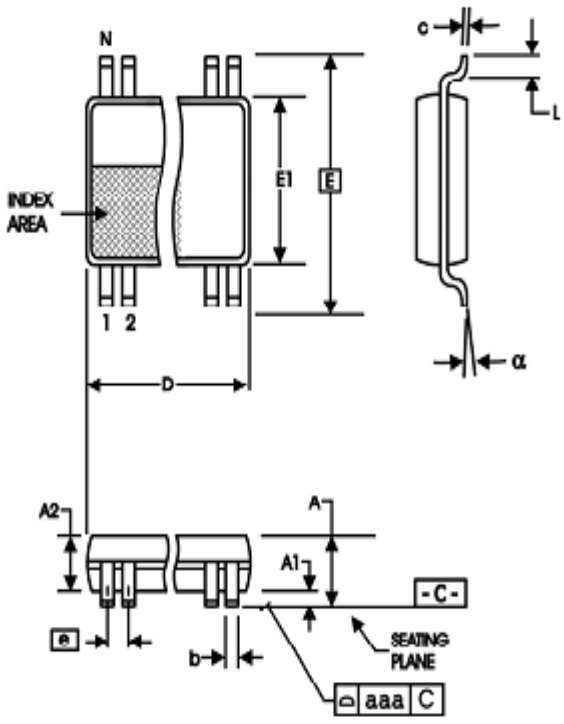
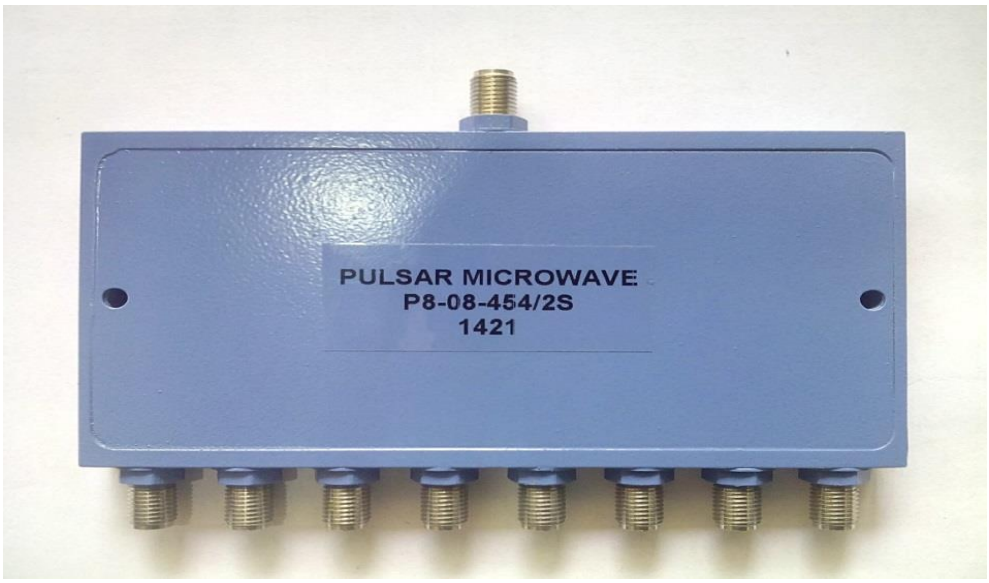


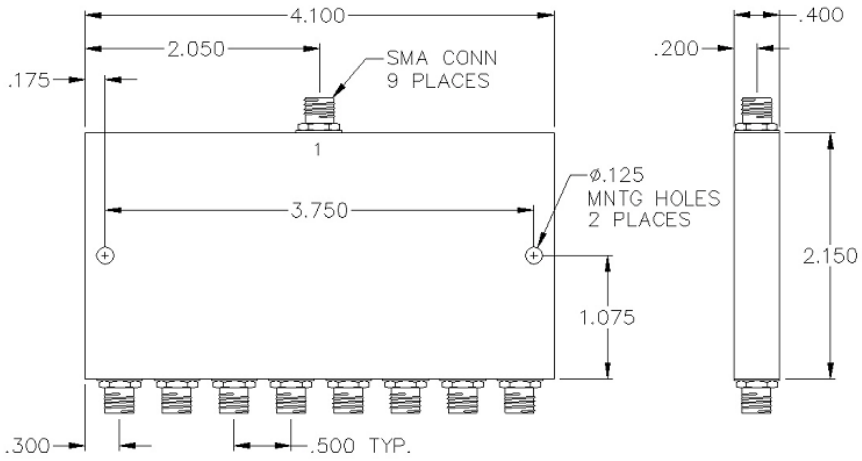
Table 7. Package Dimensions

SYMBOL	Millimeters	
	Minimum	Maximum
N	24	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	7.70	7.90
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

10.2 8 Way RF Divider (Pulsar Microwave _P8-08-454/2S):





SPECIFICATIONS

Frequency Range:	5 - 2000 MHz
Insertion Loss:	4.5 dB Max
Isolation:	16 dB Min
Amplitude Balance:	1.0 dB Max
Phase Balance:	10.0° Max
VSWR:	1.70:1 Max
Power[1]:	1 Watt Max

Notes:
1. Power rating is for load VSWR better than 1.20:1

PULSAR MICROWAVE CORPORATION

PULSAR MICROWAVE CORPORATION
48 INDUSTRIAL WEST, CLIFTON NJ 07012
TEL: 973-779-6262 FAX: 973-779-2727
WWW.PULSARMICROWAVE.COM

DESCRIPTION : 8-Way Power Divider - 0°

MODEL NO. : P8-08-454/2S

DIMENSIONS ARE IN INCHES
DECIMAL TOLERANCE:
2 PLACE ± .02
3 PLACE ± .010

SIZE A | CAGE CODE : 0HR85 | REV CODE :

SCALE : N / A | ALL SPECIFICATIONS ARE SUBJECT TO CHANGE WITHOUT NOTICE AT ANY TIME | SHEET 1 OF 1

10.3 Switch Mode Power Supply (SMPS NES-25-5) :

MEAN WELL 25W Single Output Switching Power Supply **NES-25 series**

■ Features :
- Universal AC input / Full range
- Protections: Short circuit / Overload / Over voltage
- Cooling by free air convection
- 100% full load burn-in test
- 2 years warranty

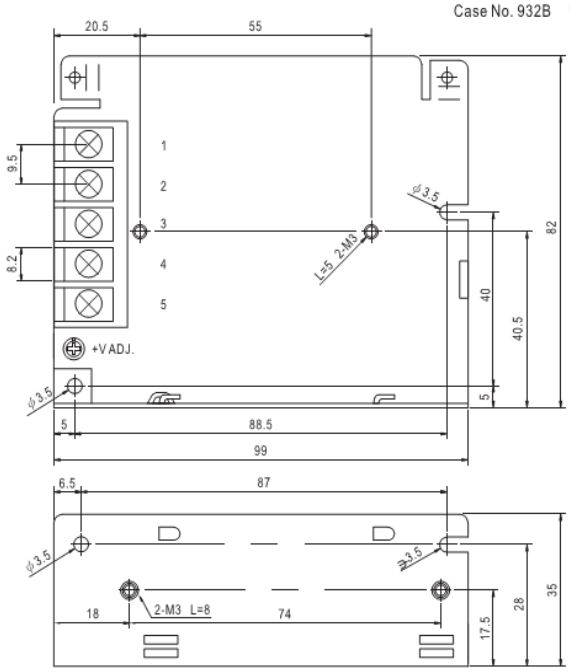
SPECIFICATION

MODEL		NES-25-5	NES-25-12	NES-25-15	NES-25-24	NES-25-48
OUTPUT	DC VOLTAGE	5V	12V	15V	24V	48V
	RATED CURRENT	5A	2.1A	1.7A	1.1A	0.57A
	CURRENT RANGE	0 ~ 5A	0 ~ 2.1A	0 ~ 1.7A	0 ~ 1.1A	0 ~ 0.57A
	RATED POWER	25W	25.2W	25.5W	26.4W	27.36W
	RIPPLE & NOISE (max.) Note.2	80mVp-p	120mVp-p	150mVp-p	200mVp-p	240mVp-p
	VOLTAGE ADJ. RANGE	4.75 ~ 5.5V	10.8 ~ 13.2V	13.5 ~ 16.5V	21.6 ~ 26.4V	43.2 ~ 52.8V
	VOLTAGE TOLERANCE Note.3	±2.0%	±1.0%	±1.0%	±1.0%	±1.0%
	LINE REGULATION Note.4	±0.5%	±0.5%	±0.5%	±0.5%	±0.5%
	LOAD REGULATION Note.5	±0.5%	±0.5%	±0.5%	±0.5%	±0.5%
	SETUP, RISE TIME	500ms, 30ms/230VAC 1200ms, 30ms/115VAC at full load				
	HOLD UP TIME (Typ.)	50ms/230VAC 10ms/115VAC at full load				
INPUT	VOLTAGE RANGE	85 ~ 264VAC 120 ~ 370VDC				
	FREQUENCY RANGE	47 ~ 63Hz				
	EFFICIENCY (Typ.)	78%	83%	84%	86%	86%
	AC CURRENT (Typ.)	0.55A/115VAC 0.35A/230VAC				
	INRUSH CURRENT (Typ.)	COLD START 45A				
	LEAKAGE CURRENT	<2mA / 240VAC				
PROTECTION	OVERLOAD	110 ~ 150% rated output power				
		Protection type : Hiccup mode, recovers automatically after fault condition is removed				
	OVER VOLTAGE	5.75 ~ 6.75V	13.8 ~ 16.2V	17.25 ~ 20.25V	27.6 ~ 32.4V	55.2 ~ 64.8V
		Protection type : Shut down o/p voltage, re-power on to recover				
ENVIRONMENT	WORKING TEMP.	-20 ~ +60°C (Refer to "Derating Curve")				
	WORKING HUMIDITY	20 ~ 90% RH non-condensing				
	STORAGE TEMP., HUMIDITY	-40 ~ +85°C, 10 ~ 95% RH				
	TEMP. COEFFICIENT	±0.03%/°C (0 ~ 45°C)				
	VIBRATION	10 ~ 500Hz, 2G 10min./1cycle, period for 60min. each along X, Y, Z axes				
SAFETY & EMC (Note 7)	SAFETY STANDARDS Note.6	UL60950-1, CB(IEC60950-1),CCC GB4943.1:2011 approved				
	WITHSTAND VOLTAGE	I/P-O/P:3KVAC I/P-FG:2KVAC O/P-FG:0.5KVAC				
	ISOLATION RESISTANCE	I/P-O/P, I/P-FG, O/P-FG:100M Ohms / 500VDC / 25°C/ 70% RH				
	EMC EMISSION	Compliance to EN55022 (CISPR22) Class B, EN61000-3-2,-3				
	EMC IMMUNITY	Compliance to EN61000-4-2, 3, 4, 5, 6, 8,11, EN55024, EN61000-6-1, light industry level, criteria A				
OTHERS	MTBF	411.47Khrs min. MIL-HDBK-217F (25°C)				
	DIMENSION	99*82*35mm (L*W*H)				
	PACKING	0.3Kg; 45pcs/14.5Kg/0.66CUFT				
NOTE	1. All parameters NOT specially mentioned are measured at 230VAC input, rated load and 25°C of ambient temperature. 2. Ripple & noise are measured at 20MHz of bandwidth by using a 12" twisted pair-wire terminated with a 0.1uf & 47uf parallel capacitor. 3. Tolerance : includes set up tolerance, line regulation and load regulation. 4. Line regulation is measured from low line to high line at rated load. 5. Load regulation is measured from 0% to 100% rated load. 6. For the request of GB4943.1,the power supply is only suitable for use in the altitude 2000m below and the non tropical climate condition. 7. The power supply is considered a component which will be installed into a final equipment. The final equipment must be re-confirmed that it still meets EMC directives. For guidance on how to perform these EMC tests, please refer to "EMI testing of component power supplies." (as available on http://www.meanwell.com)					

File Name:NES-25-SPEC 2012-09-24

Mechanical Specification

Case No. 932B Unit:mm

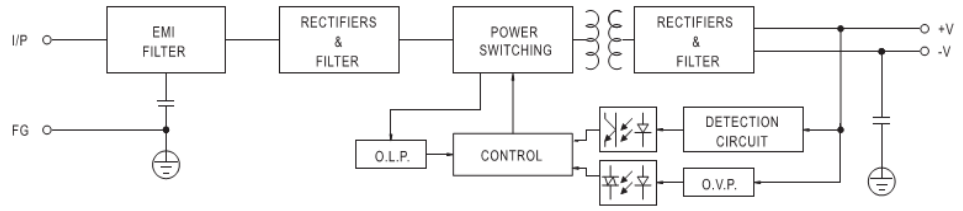


Terminal Pin No. Assignment

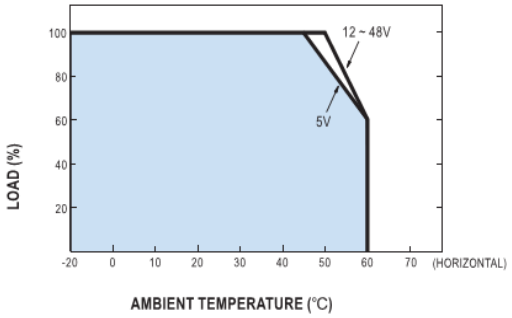
Pin No.	Assignment	Pin No.	Assignment
1	AC/L	4	DC OUTPUT -V
2	AC/N	5	DC OUTPUT +V
3	FG ⏚		

Block Diagram

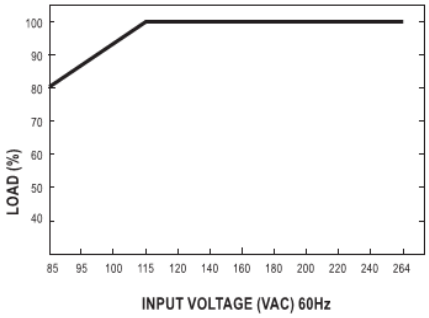
fosc : 60KHz



Derating Curve



Output Derating VS Input Voltage



File Name:NES-25-SPEC 2012-09-24