iADC Characterization Report

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iADC sampler card is a part of ROACH-I based upgrade correlator which is being used to digitize the broadband analog signals. The characterization of iADC is important in order to decide the stable operating range of FPGA back-end. This will be useful in deciding the headroom for accommodating RFI.

iADC Specifications :-

AT84AD001C Dual 8-bit 1 Gsps ADC
Vpp = 500mV
Bits = 8-bits
lsb = Vpp/2^8 = 1.953mV
Full power Input Bandwidth = 1.5 GHz (–3 dB)

For Each bit the power level required is as follows :-
Formula = [(Vpp x 2^n) / 2^8] + LSB/2

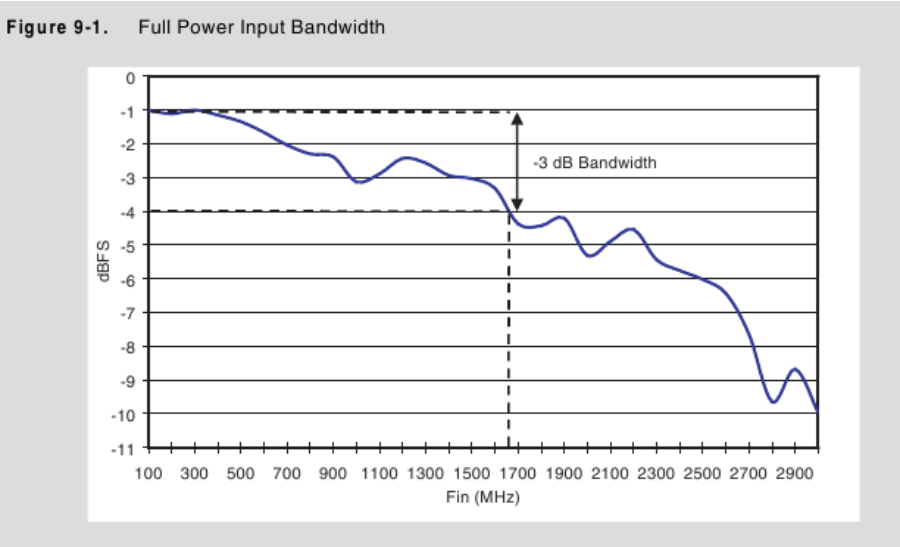
Based on above specifications, the theoretical input power required for setting each individual bit is as shown in the table below :-

Bits	**Voltage (in mV)**	**Power in (dBm) (Bitwise power)**
0000 0010	2.93	-46.684174
0000 0100	6.836	-39.324638
0000 1000	14.648	-32.704774
0001 0000	30.273	-26.399365
0010 0000	61.523	-20.239788
0100 0000	124.023	-14.150525
1000 0000	249.023	-8.095795
[1]0000 0000	499.023	-2.058181

iADC Board Losses :-

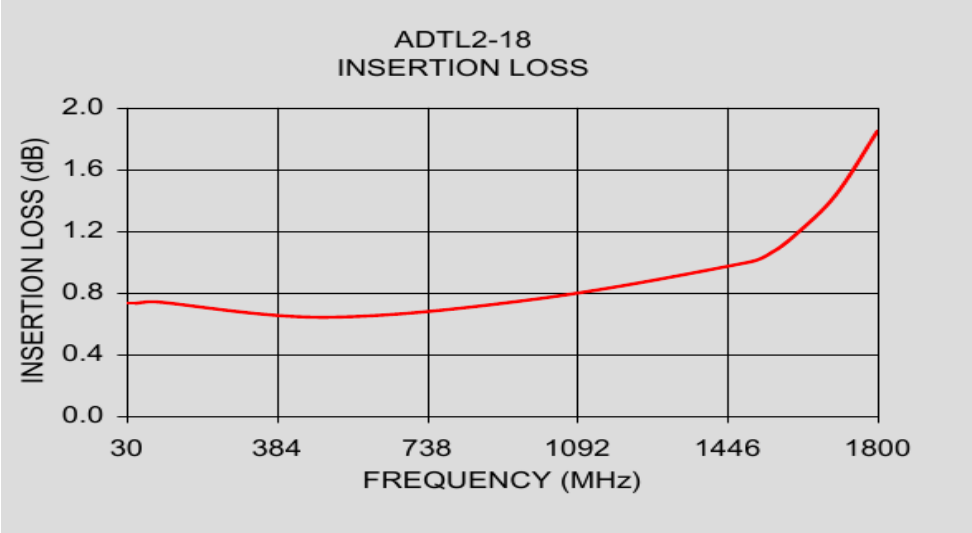
The iADC board losses are because of two components as mentioned below :-

1. ADC analog input bandwidth response is an important factor (Typical ~ 1.5 dB)



2. RF Transformer :-

   ADLT2-18 surface mount RF Transformer 50Ω 30 to 1800MHz typical characteristics :-



Incurred insertion loss ~ 0.8 dB

iADC Characterization Test Setup :-

The characterization has been carried out using lab noise source and sine wave generator.

Instruments :-

1. Micronetics Wireless Noise Generator
2. Sine wave Generator – Agilent N9310A
3. Spectrum Analyzer – Rhode & Schwarz FSP (9kHz to 7GHz)
4. 4-Antenna Packetized Correlator F-engine & Corresponding python script.

iADC Board test with noise source & sine wave :-

Characterization of iADC with sine wave can gives us a good perspective of behavior for the fundamental component of fourier transform i.e. sine wave. But characterization with noise source resembles in behavior to that of antenna signals – random in nature. Hence power of a noise signal is nothing but it's standard deviation. The spread of the distribution (in terms of standard deviation) decides the number of bits exercised in an ADC.

1. Sine wave test :- Saturated at Pin = 0.5 dBm@1.5GHz analog bandwidth of ADC
2. Noise source test :- Saturated at Pin = -16 dBm@1.5GHz analog bandwidth of ADC

Standard Deviation Test Using Noise Source:-

Design Test Setup :-

1. Design Tested :-
   Packetized Correlator–F-engine (r_128w_512_11_r370_mod3_1_2011_Nov_29_1610.bof)
2. Testing & plotting script : "corr_adc_time.py"
   The design has been modified to make it compatible with "corr_adc_time.py" script.
   This test is carried out to measure +/-3σ spread of input power level.

gmrt@rchpc3:~$ corr_adc_time.py -t 100000 -a 0x

Bits Utilized	3σ (Therotical)	3σ (Measured/adjusted)	Pin @1.5GHz (in dBm) with losses
6 to 7 bits	(64 to 127)	115 to 122	-11.09
5 to 6 bits	(32 to 63)	61 to 64	-16.62
4 to 5 bits	(16 to 31)	30 to 32	-22.54
3 to 4 bits	(8 to 15)	14.76 to 15.40	-28.54
2 to 3 bits	(4 to 7)	7.21 to 7.50	-34.95
1 to 2 bits	(2 to 3)	3.29 to 3.45	-42.06
0 to 1 bits	(0 to 1)	1.65	-50.30

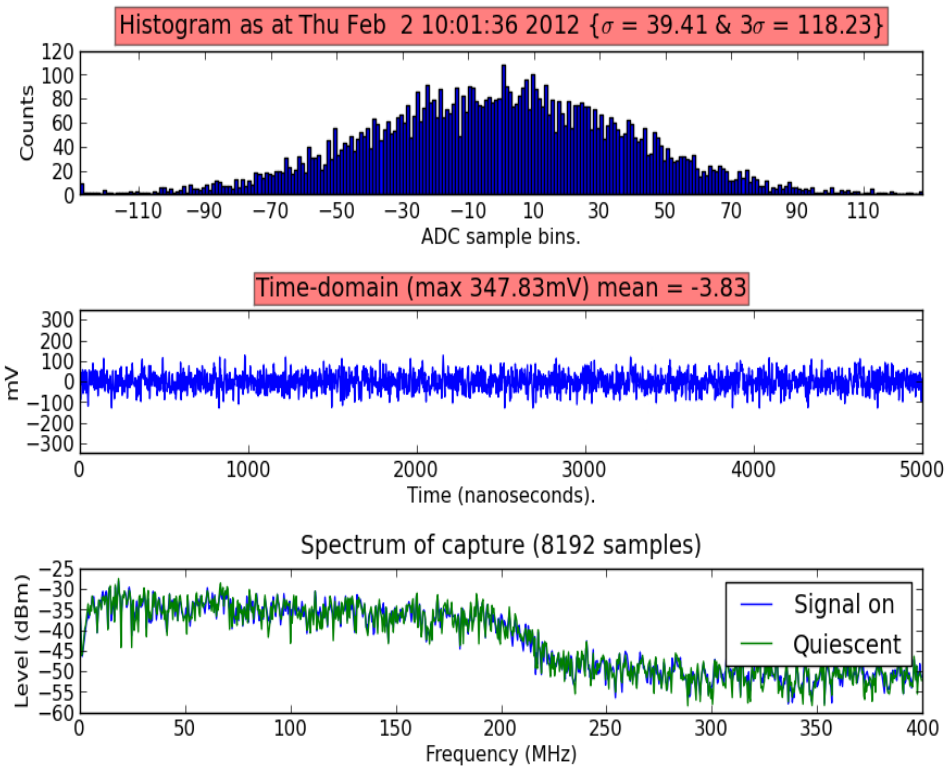


Fig 1: iADC 6 to 7-bits utilization Histogram

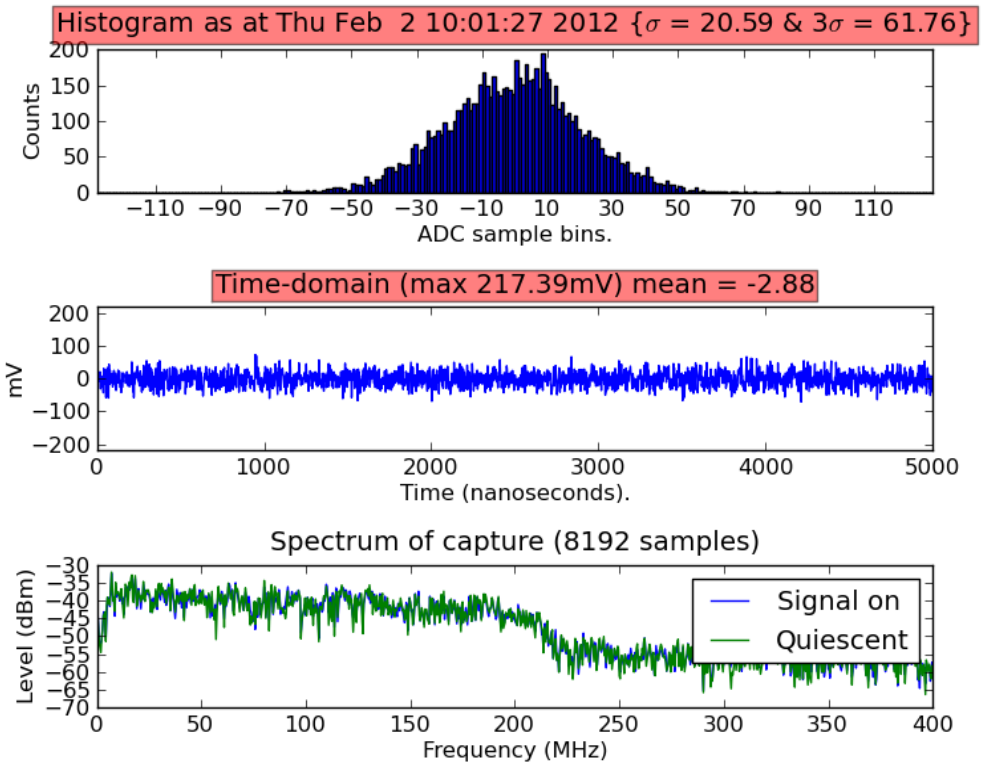


Fig 2: iADC 5 to 6-bits utilization Histogram

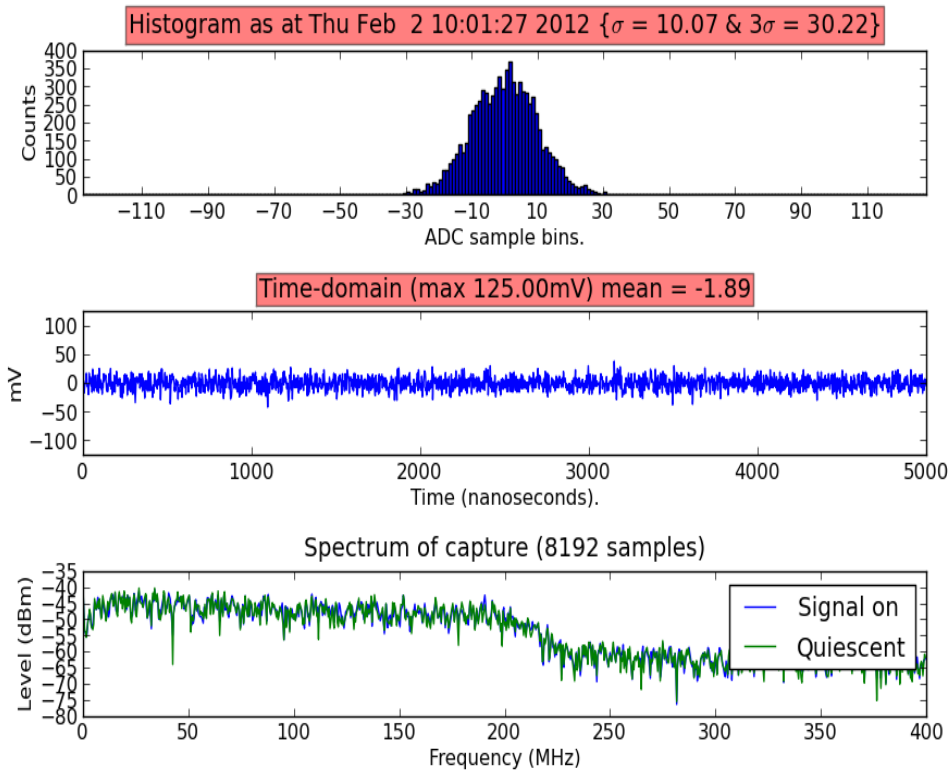


Fig 3: iADC 4 to 5-bits utilization Histogram

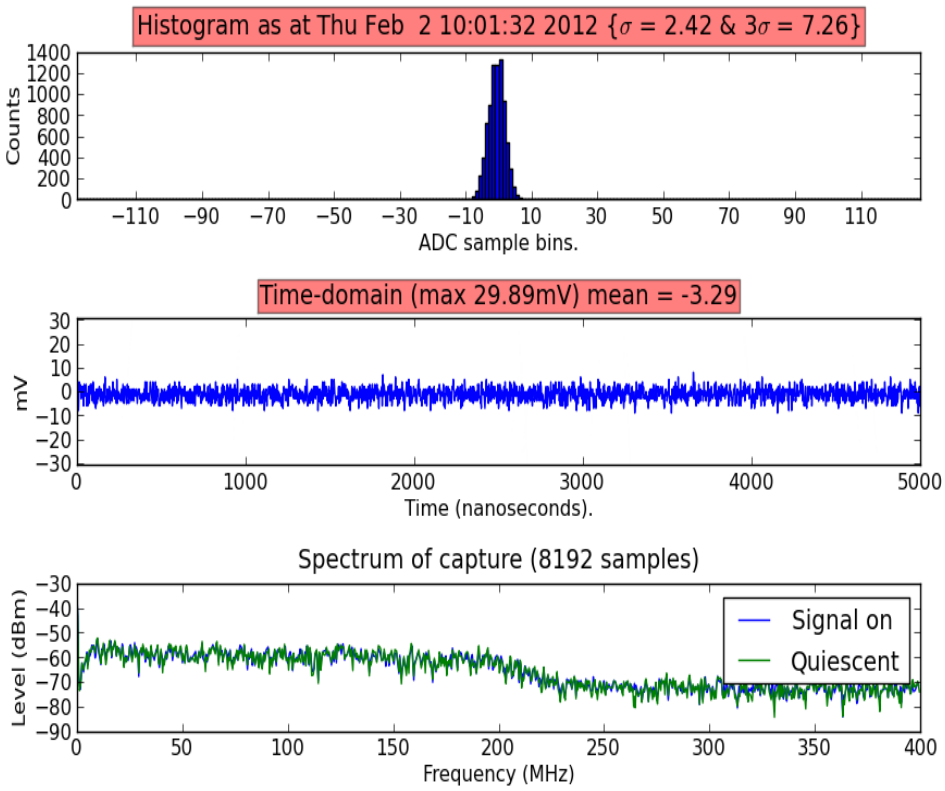


Fig 4: iADC 4 to 3-bits utilization Histogram

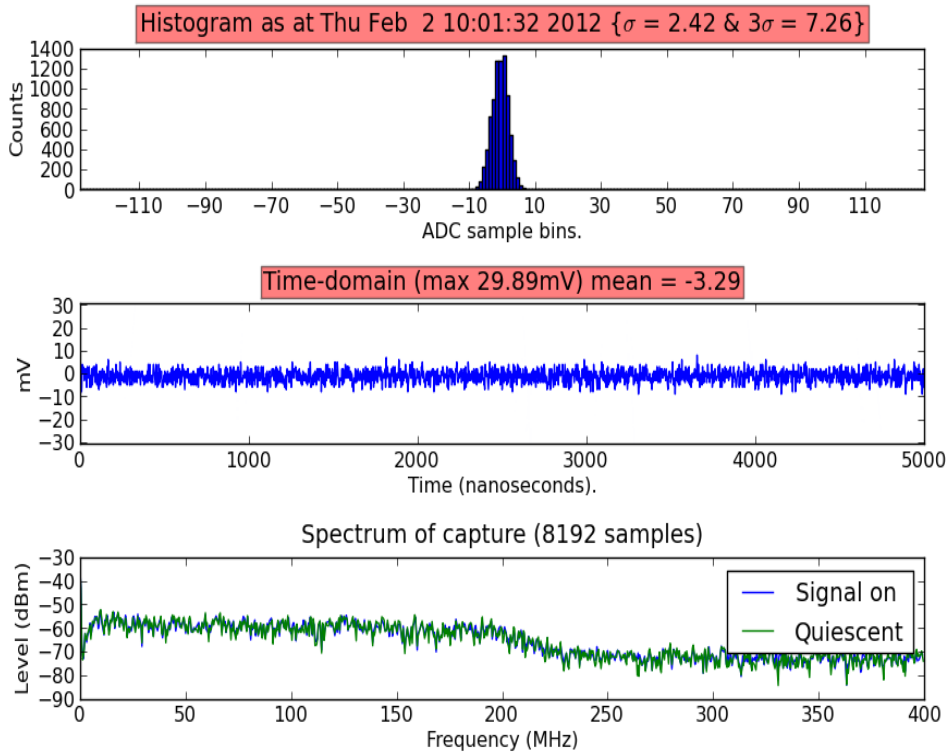


Fig 5: iADC 3 to 2-bits utilization Histogram

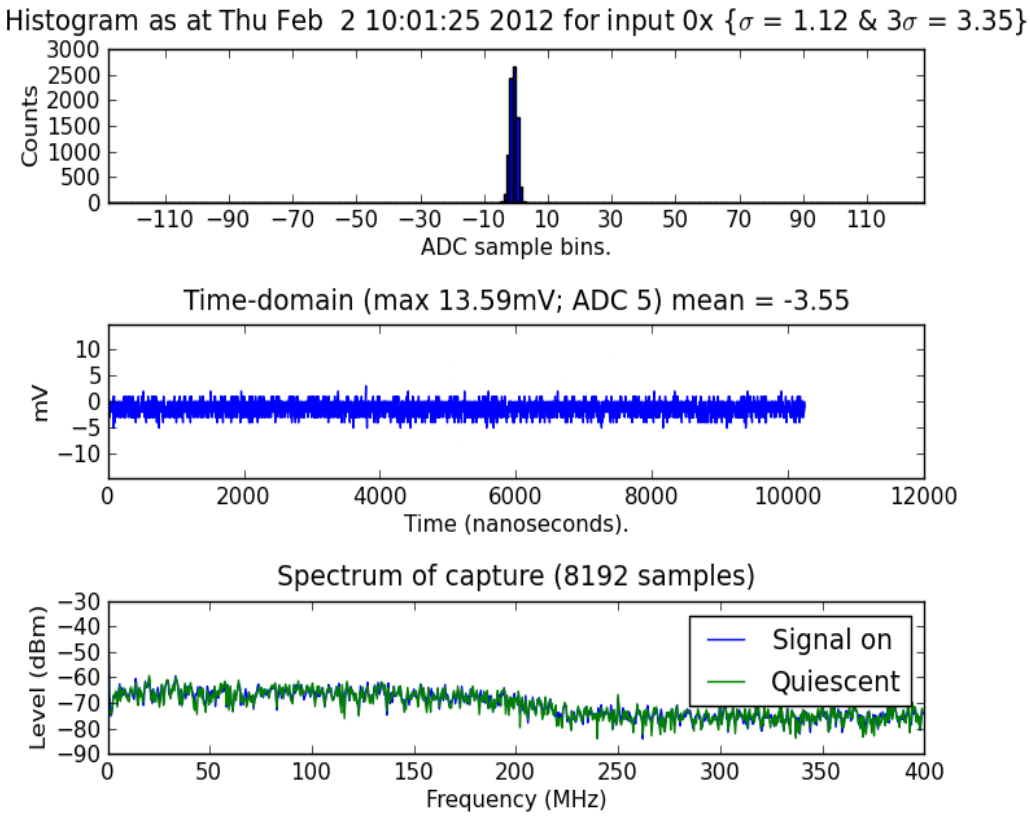


Fig 6: iADC 2 to 1-bits utilization Histogram

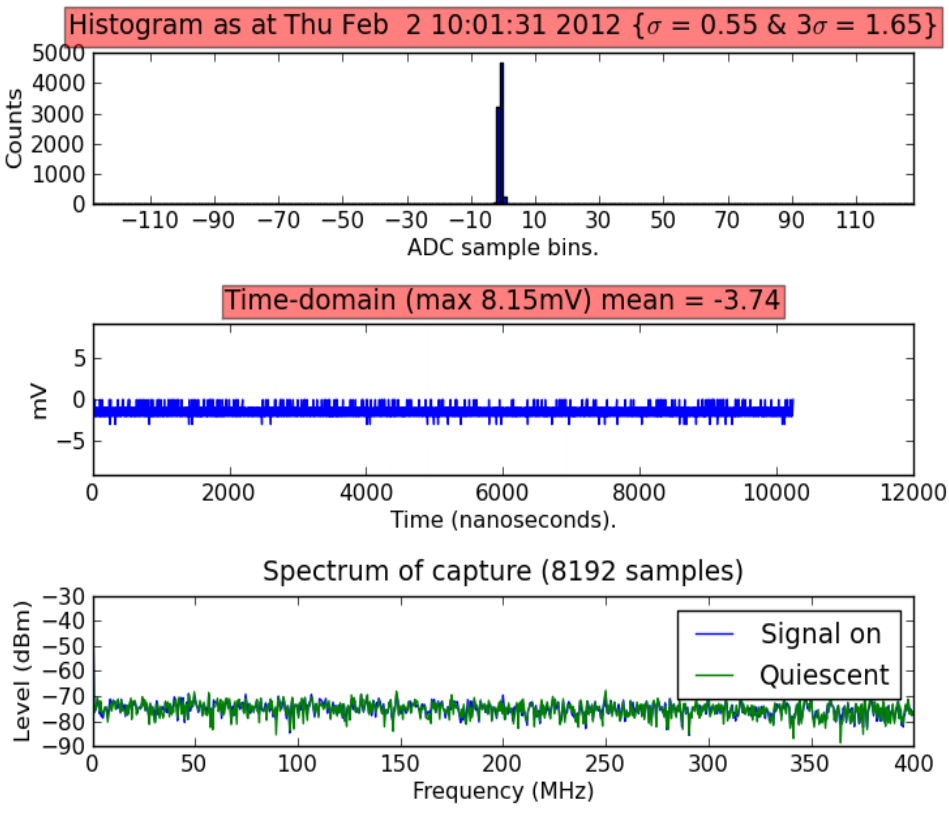


Fig 7: iADC 0 to 1-bits utilization Histogram

Conclusion :-

iADC characterization test were carried out for sine wave and noise inputs to determine range of operation of ADC for stable operation of digital back-end. After providing 1-bit headroom for RFI, the optimal noise input power over the analog bandwidth of ADC should be in the range of (-16.7dBm to -22.5dBm).

The ADC saturates at -11.2dBm power level over analog bandwidth of ADC.

References :-

1. AT84AD001C ADC Datasheet
2. ADLT2-18 RF transformer Datasheet

Version History :-

1. Version 1 : Initial Version 2nd February 2012
2. Version 2 : Details about test setup and conclusion 30th March 2012